NOVATEK
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Data Sheet

NT35510 – General Specification

One-chip Driver IC with internal GRAM
for 16.7M colors 480RGB x 864 a-Si TFT LCD
with CPU / RGB / MIPI / MDDI Interface

V0.00

Preliminary

REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Original	Kevin	SW	Dennis	2010/11/3

1 DESCRIPTION

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35510. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

The NT35510 device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 480RGBx864, 480RGBx854, 480RGBx800, 480RGBx720, 480RGBx640 with internal CGRAM. It includes a 9,953,280 bits internal memory, a timing controller with glass interface level-shifters and a glass power supply circuit..

The NT35510 supports MDDI interface, MIPI Interface, 16/18/24 bits RGB interface, 8/16/24-bit system interfaces, serial peripheral interfaces (SPI) and I2C interface. The specified window area can be updated selectively, so that moving pictures can be displayed simultaneously independent of the still picture area.

The NT35510 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities. The IC possesses internal GRAM that stores 480-RGB x 864-dot 16.77M-color images. A deep standby mode is also supported for lower power consumption.

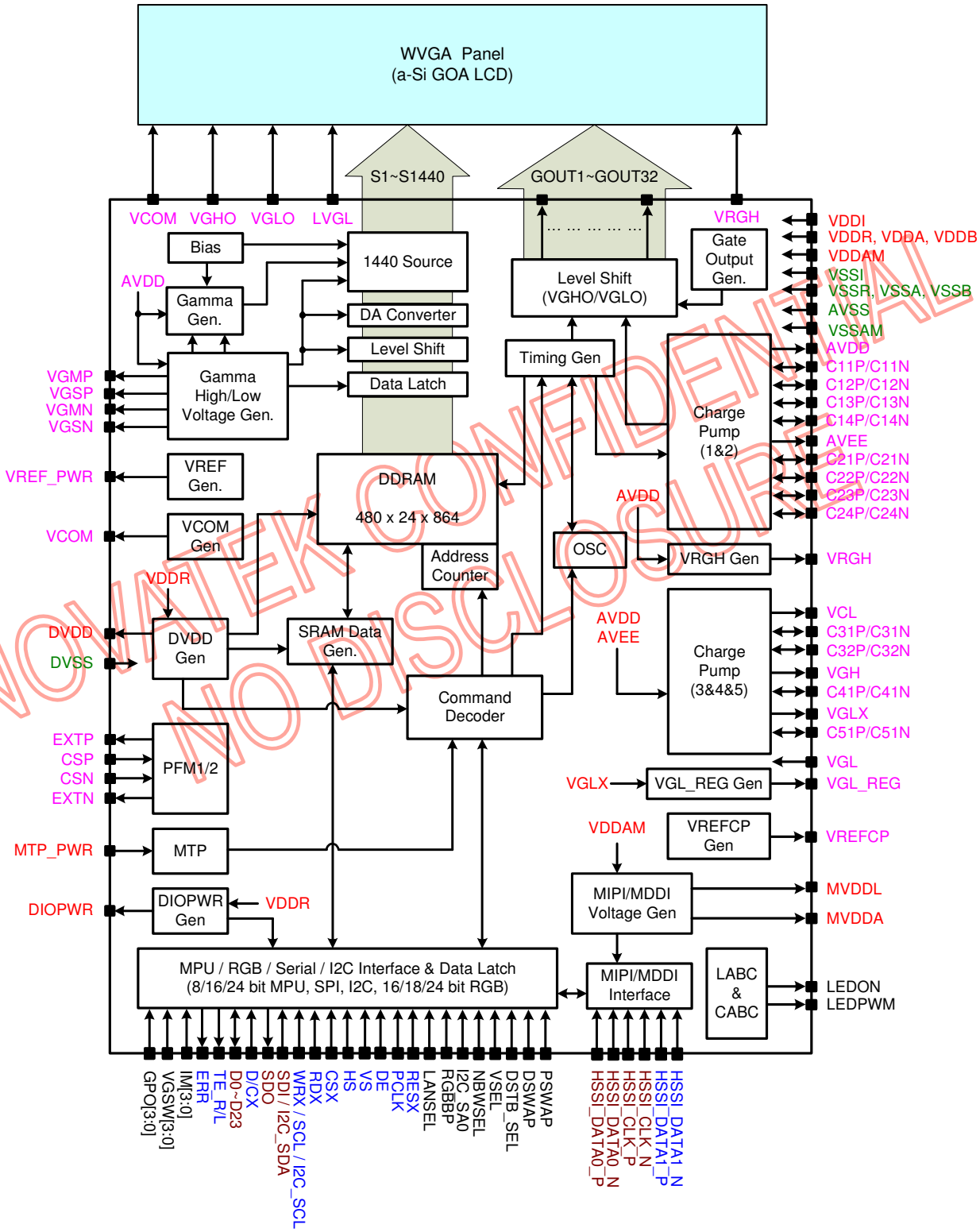
This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA..

2 FEATURES

- Single chip WVGA a-Si TFT LCD Controller/driver with Display RAM.
- Display resolution option
  - 480RGB x 864 with 480x24-bitsx 864 GRAM
  - 480RGB x 854 with 480x24-bitsx 854 GRAM
  - 480RGB x 800 with 480x24-bitsx 800 GRAM
  - 480RGB x 720 with 480x24-bitsx 720 GRAM
  - 480RGB x 640 with 480x24-bitsx 640 GRAM
- Display data RAM (frame memory): 480 x 864 x 24-bits = 9,953,280 bits
- Display mode (Color mode)
  - Full color mode: 16.7M-colors
  - Reduce color mode: 262K colors
  - Reduce color mode: 65K colors
  - Idle mode: 8-colors
- Interface
  - 8-/16-/24-bits 80-series MPU interface
  - 16-bit serial peripheral interface
  - I2C interface
  - 16-/18-/24-bits RGB interface (DE mode and SYNC mode with polarity of HS/VS can be set by register)
  - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 1 or 2 data lane pairs)
  - Mobile Display Digital Interface (MDDI V1.2, 1 strobe and 1 or 2 data lane pairs)
- Display features
  - Window address functions for specifying a rectangular area on the internal RAM to write data
  - Individual gamma correction setting for RGB dots
  - Deep standby function
- On chip
  - VGHO/VGLO voltage generator for gate control signal and panel
  - Oscillator for display clock
  - Supports gate control signals to gate driver in the panel
  - On module color characteristics
  - On module checksums checking
  - Four GPO (General Purpose Output) pins for external control
- Supply voltage range
  - I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.3V (VDDI) or 1.1 ~ 1.3V (VDDIL)
  - Analog supply voltage range for VDDB/VDDA/VDDR to VSSB/VSSA/VSSR: 2.3V ~ 4.8V
  - MIPI/MDDI regulator supply voltage range for VDDAM to VSSAM: 2.3V ~ 4.8V

◆ Output voltage levels
- Positive gate driver voltage range for VGH: AVDD+VDDB ~ 2xAVDD - AVEE
- Negative gate driver voltage range for VGLX: AVEE+VCL ~ 2xAVEE-AVDD
- Step-up 1 output voltage range for AVDD: 4.5 ~ 6.5V
- Step-up 2 output voltage range for AVEE: -4.5 ~ -6.5V
- Positive gamma high voltage range for VGMP: 3.0 ~ 6.3V (AVDD-0.3V)
- Positive gamma low voltage range for VGSP: 0.0, 0.3 ~ 3.7V
- Negative gamma high voltage range for VGMN: -3.0 ~ -6.3V (AVEE+0.3V)
- Negative gamma low voltage range for VGSN: 0.0, -0.3 ~ -3.7V
- Common electrode voltage range for VCOM: 0.0 ~ -3.5V (VCL+0.3V)
- Panel voltage range for VRGH: 1.0V ~ 6.0V(AVDD-0.3V)

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1 Power Supply Pins

Symbol	Name	Description
VDDB	DC/DC Power	Power supply for DC/DC converter VDDB, VDDA and VDDR should be the same input voltage level
VDDA	Analog Power	Power supply for analog system VDDB, VDDA and VDDR should be the same input voltage level
VDDR	Regulator Power	Power supply for regulator system VDDB, VDDA and VDDR should be the same input voltage level
VDD_DET	Detection Power	Connect to VDDB/VDDA/VDDR for detection.
VDDAM	MIPI Power	Power supply for MIPI/MDDI analog regulator system
VDDI	I/O Power	Power supply for interface system except MIPI/MDDI interface
DVDD	Digital Voltage	Regulator output for logic system power (1.55V typical) Connect a capacitor for stabilization.
DIOPWR	Dual I/O Voltage	Regulator output for dual I/O voltage system (1.2V/1.8V typical). Connect a capacitor for stabilization.
MVDDA	MIPI/MDDI Voltage	Regulator output for internal MIPI/MDDI analog system (1.5V typical) Connect a capacitor for stabilization. If not use MIPI/MDDI interface, please open this pin.
MVDDL	MIPI Voltage	Regulator output for internal MIPI low power system (1.2V typical) Connect a capacitor for stabilization. If not use MIPI interface, please open this pin
VSSB	DC/DC GND	System ground for DC/DC converter
VSSA	Analog GND	System ground for analog system
VSSR	Regulator GND	System ground for regulator system
VSSAM	MIPI GND	System ground for internal MIPI/MDDI analog system
VSSI	I/O GND	System ground for interface system except MIPI/MDDI interface
DVSS	Digital GND	System ground for internal digital system
AVSS	Source OP GND	System ground for source OP system.
MTP_PWR	MTP Power	MTP programming power supply pin (7.5 to 8.0V and 7.75V typical) Must be left open or connected to DVSS in normal condition.

4.2 80-System Interface Pins

Symbol	I/O	Description
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	WRX: Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
RDX	I	Reads strobe signal to write data when RDX is “Low” in 80-series MPU interface. This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D/CX	I	Display data / command selection in 80-series MPU I/F. D/CX = ”0” : Command D/CX = ”1” : Display data or Parameter This pin is not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F. For 8080-series MPU I/F: 8-bit interface: D[7:0] are used, D[23:8] should be connected to VSSI 16-bit interface: D[15:0] are used, D[23:16] should be connected to VSSI 24-bit interface: D[23:0] are used These pins are not used for 16-bit SPI, I2C, MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: “1” = VDDI level, “0” = VSSI level.

4.3 SPI /I2C Interface Pins

Symbol	I/O	Description
CSX	I	Chip select input pin (“Low” enable) in 80-series MPU I/F and SPI I/F. This pin is not used for I2C, MIPI or MDDI I/F, please connect to VSSI this pin.
WRX / SCL / I2C_SCL	I	Writes strobe signal to write data when WRX is “Low” in 80-series MPU I/F. SCL: A synchronous clock signal in SPI I/F. I2C_SCL: Serial input clock in I2C I/F. This pin is not used for MIPI I/F, please connect to VSSI this pin.
SDI / I2C_SDA	I/O	SCL: Serial input signal in SPI I/F. The data is input on the rising/falling edge of the SCL signal. I2C_SDA: Serial input/output signal in I2C I/F. The data is input/output on the rising edge of the I2C_SCL signal. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
SDO	O	Serial output signal in SPI I/F. The data is output on the rising/falling edge of the SCL signal. If the host places the SDI line into high-impedance state during the read interval, the SDI and SDO can be tied together. This pin is not used for 80-series MPU, I2C, MIPI or MDDI I/F, please open this pin.

NOTE: “1” = VDDI level, “0” = VSSI level.

4.4 RGB Interface Pins

Symbol	I/O	Description
PCLK	I	Pixel clock signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
VS	I	Vertical sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
HS	I	Horizontal sync. Signal in RGB I/F. This pin is not used for 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
DE	I	Data enable signal in RGB I/F mode 1. This pin is not used for RGB mode 2, 80-series MPU, MIPI or MDDI I/F, please connect to VSSI this pin.
D[23:0]	I/O	24-bit bi-directional data bus for 80-series MPU I/F and 24-bit input data bus for RGB I/F.. For RGB I/F: 16-bit/pixel: D[20:16]=R[4:0], D[13:8]=G[5:0] and D[4:0]=B[4:0], connect unused pins to VSSI 18-bit/pixel: D[21:16]=R[5:0], D[13:8]=G[5:0] and D[5:0]=B[5:0], connect unused pins to VSSI 24-bit/pixel: D[23:16]=R[7:0], D[15:8]=G[7:0] and D[7:0]=B[7:0] These pins are not used for MIPI or MDDI I/F, please connect to VSSI these pins.

NOTE: "1" = VDDI level, "0" = VSSI level.

4.5 MIPI/MDDI Interface Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>HSSI_CLK_P
HSSI_CLK_N</td><td>I</td><td>-These pins are DSI-CLK+/- differential clock signals if MIPI interface is used.
-These pins are MDDI_STB_P/M differential strobe signals if MDDI interface is used.
-HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D0_P
HSSI_D0_N</td><td>I/O</td><td>-These pins are DSI-D0+/- differential data signals if MIPI interface is used.
-These pins are MDDI_DATA0_P/M differential strobe signals if MDDI interface is used.
-HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>HSSI_D1_P
HSSI_D1_N</td><td>I</td><td>-These pins are DSI-D1+/- differential data signals if MIPI interface is used.
-These pins are MDDI_DATA1_P/M differential strobe signals if MDDI interface is used.
-HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm.
-If not used, please connect these pins to VSSAM.</td></tr>
<tr><td>ERR</td><td>O</td><td>CRC and ECC error output pin for MIPI interface. This pin is output low when it is not activated.
When this pin is activated, it output high if CRC/ECC error found.
If not used, please open this pin.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>Input pin to select 1 data lane or 2 data lanes in MIPI/MDDI interface.
<table>
<tr><th>LANSEL</th><th>Data Lane of MIPI/MDDI</th></tr>
<tr><td>0</td><td>1 data lane</td></tr>
<tr><td>1</td><td>2 data lanes</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>Input pin to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only.
For MIPI interface, both DSWAP and PSWAP function are available.
For MDDI interface, only PSWAP function is available. Please connect DSWAP pin to VSSI.
<table>
<tr><th colspan="2">Pin Name</th><th>HSSI_D0_P</th><th>HSSI_D0_N</th><th>HSSI_CLK_P</th><th>HSSI_CLK_N</th><th>HSSI_D1_P</th><th>HSSI_D1_N</th></tr>
<tr><td rowspan="4">Input MIPI Signal</td><td>DSWAP=0
PSWAP=0</td><td>DSI-D0+</td><td>DSI-D0-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D1+</td><td>DSI-D1-</td></tr>
<tr><td>DSWAP=0
PSWAP=1</td><td>DSI-D0-</td><td>DSI-D0+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D1-</td><td>DSI-D1+</td></tr>
<tr><td>DSWAP=1
PSWAP=0</td><td>DSI-D1+</td><td>DSI-D1-</td><td>DSI-CLK+</td><td>DSI-CLK-</td><td>DSI-D0+</td><td>DSI-D0-</td></tr>
<tr><td>DSWAP=1
PSWAP=1</td><td>DSI-D1-</td><td>DSI-D1+</td><td>DSI-CLK-</td><td>DSI-CLK+</td><td>DSI-D0-</td><td>DSI-D0+</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
</table>

4.6 Interface Logic Pins

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESX</td><td>I</td><td>
This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.
The input voltage range for RESX pin is related to DSTB_SEL and VSEL pins.
<table>
<tr><th colspan="2">Input Voltage Level (DSTB_SEL="0")</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td rowspan="2">VDDI=1.65~3.3V</td><td>Logic High level input voltage</td><td>0.7xVDDI</td><td>VDDI</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td><td>V</td></tr>
<tr><td rowspan="2">VDDI=1.1~1.3V</td><td>Logic High level input voltage</td><td>0.88</td><td>1.35</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
<table>
<tr><th colspan="2" rowspan="2">Input Voltage Level (DSTB_SEL="1")</th><th colspan="2">VDDI=1.65~3.3V</th><th colspan="2">VDDIL=1.1~1.3V</th><th rowspan="2">Unit</th></tr>
<tr><th>Min.</th><th>Max.</th><th>Min.</th><th>Max.</th></tr>
<tr><td rowspan="2">VSEL =High</td><td>Logic High level input voltage</td><td>0.7xVDDI</td><td>VDDI</td><td>1.155</td><td>1.95</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.3xVDDI</td><td>VSSI</td><td>0.585</td><td>V</td></tr>
<tr><td rowspan="2">VSEL =Low</td><td>Logic High level input voltage</td><td>0.88</td><td>1.35V</td><td>0.88</td><td>1.35V</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
</td></tr>
<tr><td>TE
(TE_L)</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
When this pin is not activated, this pin is output low.
If not used, please open this pin.</td></tr>
<tr><td>TE_R</td><td>O</td><td>Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command.
The same output signal as TE (TE_L) pin.
If not used, please open this pin.</td></tr>
<tr><td>IM[3:0]</td><td>I</td><td>
Interface type selection. The connections of IM[3:0] which not shown in table are invalid.
<table>
<tr><th>IM[3:0]</th><th>Display Data</th><th>Command</th></tr>
<tr><td>0000</td><td>80-series 8-bit MPU I/F, D[7:0]</td><td>80-series 8-bit MPU I/F, D[7:0]</td></tr>
<tr><td>0001</td><td>80-series 16-bit MPU I/F, D[15:0]</td><td>80-series 16-bit MPU I/F, D[15:0]</td></tr>
<tr><td>0010</td><td>80-series 24-bit MPU I/F, D[23:0]</td><td>80-series 24-bit MPU I/F, D[23:0]</td></tr>
<tr><td>0011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>1011</td><td>RGB I/F, D[23:0]</td><td>16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0100</td><td>RGB I/F, D[23:0]</td><td>I2C I/F, I2C_SDA</td></tr>
<tr><td>0101</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MIPI DSI,
HSSI_D0_P/N, HSSI_D1_P/N</td></tr>
<tr><td>0110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL rising edge trigger), SDI/SDO</td></tr>
<tr><td>1110</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
16-bit SPI (SCL falling edge trigger), SDI/SDO</td></tr>
<tr><td>0111</td><td>MDDI,
HSSI_D0_P/N, HSSI_D1_P/N</td><td>MDDI, HSSI_D0_P/N, HSSI_D1_P/N
I2C I/F, I2C_SDA serial data</td></tr>
</table>
</td></tr>
<tr><td>RGBBP</td><td>I</td><td>Display data written path control in RGB interface.
RGBBP="0", display data written to frame memory.
RGBBP="1", display data written to line buffer (frame memory by pass mode)
When not used in other interfaces, please connect to VSSI.</td></tr>
</table>

<table>
<tr><td>I2C_SA0</td><td>I</td><td>Select the I2C interface address from MPU. If not used, please connect to VSSI.
<table>
<tr><th>I2C_SA0</th><th>Slave Address</th></tr>
<tr><td>0</td><td>10011 00</td></tr>
<tr><td>1</td><td>10011 01</td></tr>
</table></td></tr>
<tr><td>VSEL</td><td>I</td><td>Input pin to switch the I/O voltage.
This VSEL function only apply for RESX, TE, LEDPWM, LEDON, KBBC pins.
The VSEL dual IO function is valid when DSTB_SEL=”1”.
<table>
<tr><th rowspan="2">DSTB_SEL</th><th rowspan="2">VDDI</th><th rowspan="2">VSEL</th><th rowspan="2">DIOPWR</th><th colspan="2">Output Voltage Level</th></tr>
<tr><th>TE</th><th>LEDON
LEDPWM</th></tr>
<tr><td>0</td><td>1.65~3.3V
or
1.1~1.3V</td><td>X</td><td>Off</td><td>VOH=VDDI
VOL=VSSI</td><td>VOH=VDDI or VDDA
VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.65~3.3V</td><td>Low</td><td>1.2V</td><td>VOH=1.2V
VOL=VSSI</td><td>VOH=1.2V
VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8V</td><td>VOH=VDDI or DIOPWR
VOL=VSSI</td><td>VOH=VDDI or VDDA
VOL=VSSI</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">1.1~1.3V</td><td>Low</td><td>1.2V</td><td>VOH=1.2V
VOL=VSSI</td><td>VOH=1.2V
VOL=VSSI</td></tr>
<tr><td>High</td><td>1.8V</td><td>VOH=1.8V
VOL=VSSI</td><td>VOH=1.8V
VOL=VSSI</td></tr>
</table>
The input voltage range for VSEL pin:
<table>
<tr><th>Input Voltage Level</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>Logic High level input voltage</td><td>0.88</td><td>VDDI</td><td>V</td></tr>
<tr><td>Logic Low level input voltage</td><td>VSSI</td><td>0.55</td><td>V</td></tr>
</table>
If not used, please connect to VDDI.</td></tr>
<tr><td>GPO[3:0]</td><td>O</td><td>General purpose output pins. The output voltage swing is VDDI to VSSI.
If not used, please open these pins.</td></tr>
<tr><td>VGSW[3:0]</td><td>I</td><td>Input pin to select the different application.</td></tr>
<tr><td>EXB1T</td><td>I</td><td>Input pin to select the external AVDD DC/DC voltage.
<table>
<tr><th>EXB1T</th><th>AVDD Voltage</th></tr>
<tr><td>0</td><td>Use internal DC/DC for AVDD</td></tr>
<tr><td>1</td><td>Use external DC/DC for AVDD</td></tr>
</table>
If not used, please connect to VSSI.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>Input pin to select the voltage sequence of V0 ~ V255.
<table>
<tr><th>NBWSEL</th><th>V0 ~ V255 voltage sequence</th></tr>
<tr><td>0</td><td>$V_{(00h)}>V_{(01h)}>\ldots>V_{(FEh)}>V_{(FFh)}$ (Normally White)</td></tr>
<tr><td>1</td><td>$V_{(00h)}<V_{(01h)}<\ldots<V_{(FEh)}<V_{(FFh)}$ (Normally Black)</td></tr>
</table></td></tr>
<tr><td>DSTB_SEL</td><td>I</td><td>Input pin to control DIOPWR regulator on/off.
<table>
<tr><th>DSTB_SEL</th><th>DIOPWR Regulator</th><th>VSEL Function</th></tr>
<tr><td>0</td><td>DIOPWR Off</td><td>Invalid</td></tr>
<tr><td>1</td><td>DIOPWR On</td><td>Valid</td></tr>
</table></td></tr>
</table>

NOTE: “1” = VDDI level, “0” = VSSI level.

4.7 Driver Output Pins

Symbol	I/O	Description
S1 ~ S1440	O	Pixel electrode driving output.
GOUT1 ~ GOUT32	O	Gate control signals for panel. The swing voltage level is VGHO to VGLO
SDUM0~3	O	Dummy Source, leave it Open if not used
VGHO	O	High voltage level for gate control signals and gate circuit of panel.
VGLO	O	Low voltage level for gate control signals and gate circuit of panel.
LVGL	O	Low voltage level for gate circuit of panel.
VCOM	O	Regulator output for common voltage of panel. Connect a capacitor for stabilization.

4.8 DC/DC Converter Pins

Symbol	I/O	Description
AVDD	O	Output voltage from step-up circuit 1, generated from VDDB. Connect a capacitor for stabilization.
AVEE	O	Output voltage from step-up circuit 2, generated from VDDB. Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from VDDB. Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGLX	O	Output voltage from step-up circuit 5. Connect a capacitor for stabilization.
VGL	I	Substrate voltage for driver IC. Please connect VGL to VGLX.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	O	Capacitor connection pins for the step-up circuit which generate AVDD. Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	O	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement.
C41P, C41N	O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	O	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
VRGH	O	Output voltage generated from AVDD. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG	O	Output voltage generated from VGLX. LDO output used for panel voltage. Connect a capacitor for stabilization. When not in use, please open this pin.
EXTP	O	PFM1 control output for DC/DC converter to generate AVDD. Connect to gate of external NMOS device. When not in use, please open this pin.
EXTN	O	PFM2 control output for DC/DC converter to generate AVEE. Connect to gate of external PMOS device. When not in use, please open this pin.
CSP	I	Current sensing input for PFM1 DC/DC converter (generate AVDD). When not in use, please connect to VSSB.
CSN	I	Current sensing input for PFM2 DC/DC converter (generate AVEE). When not in use, please connect to VSSB.
VREF_PWR	O	Regulator output for power voltage. Connect a capacitor for stabilization.
VREFCP	O	Reference voltage for internal voltage generating circuit. Connect capacitor for stabilization.

Symbol	I/O	Description
VGMP	O	Output voltage generated from AVDD. LDO output for positive gamma high voltage generator.
VGSP	O	Output voltage generated from AVDD. LDO output for positive gamma low voltage generator.
VGMN	O	Output voltage generated from AVEE. LDO output for negative gamma high voltage generator.
VGSN	O	Output voltage generated from AVEE. LDO output for negative gamma low voltage generator.

4.9 LABC and CABC Control Pins

Symbol	I/O	Description
LEDON	O	This pin is connect to the external LED driver. It is a LED driver control signal which is used for turning ON/OFF the LED backlight. If not used, please open this pin.
LEDPWM	O	This pin is connect to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.

4.10 Test Pins

Symbol	I/O	Description
PADA1 PADA2 PADA3 PADA4 PADB1 PADB2 PADB3 PADB4	I/O	- These test pins for chip attachment detection. PADA1 to PADA4 are output pins and PADB1 to PADB4 are input pins. - For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace. Connect PADA3 and PADB3 together by ITO trace. Connect PADA4 and PADB4 together by ITO trace.
CONTACT1A, CONTACT1B, CONTACT2A, CONTACT2B	I/O	- Test pin, for test bonding quality, IC internal will connect CONTACT1A with CONTACT1B, CONTACT2A with CONTACT2B
AVSS_AVDD	I	Test pin, must be connected to AVSS
AVEE_AVSS	I	Test pin, must be connected to AVEE
VCL_VDDB	I	Test pin, must be connected to VCL
VCL_AVSS	I	Test pin, must be connected to VCL
VGMN_VGMP	I	Test pin, must be connected to VGMN
VGSN_VGSP	I	Test pin, must be connected to VGSN
KBBC	O	Test pin, not accessible to user. Must be left open.
TEST0~7	I/O	Test pin, not accessible to user. Must be left open.
OSC_TEST	I/O	Test pin, not accessible to user, Must left open
VDDI_OPT1~2	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSI_OPT1	O	Use them to fix the electrical potentials of unused interface pins and fixed pins. When not in use, leave it open.
VSSIDUM0~106	O	-These pins are dummy with VSSI potential (not have any function inside). -Signal traces can't pass through on glass under these pads.

5 FUNCTIONAL DESCRIPTION

5.1 MPU Interface

NT35510 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM3, IM2, IM1 and IM0 pins as show in ***Table 5.1.1***

Table 5.1.1 Interface Type Selection

IM3	IM2	IM1	IM0	SRAM	Register
0	0	0	0	80-series 8-bit MPU interface, D[7:0]	80-series 8-bit MPU interface, D[7:0]
0	0	0	1	80-series 16-bit MPU interface, D[15:0]	80-series 16-bit MPU interface, D[15:0]
0	0	1	0	80-series 24-bit MPU interface, D[23:0]	80-series 24-bit MPU interface, D[23:0]
0	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL rising trigger
1	0	1	1	RGB interface, D[23:0]	16-bit SPI, SDI/SDO serial data, SCL falling trigger
0	1	0	0	RGB interface, D[23:0]	I2C interface, I2C_SDA serial data
0	1	0	1	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D1_P/N
0	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL rising trigger
1	1	1	0	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N SPI, SDI/SDO serial data, SCL falling trigger
0	1	1	1	MDDI, HSSI_D0_P/N, HSSI_D1_P/N	MDDI, HSSI_D0_P/N, HSSI_D1_P/N I2C interface, I2C_SDA serial data

Note: "X" = Don't care.

5.1.2 80-series MPU Interface

The MCU uses an 11-wires 8-data or 19-wires 16-data or 27-wires 24-data parallel interface.
The chip-select CSX (active low) enables and disables the parallel interface. WRX is the parallel data write, RDX is the parallel data read and D[23:0] is parallel data.

The Graphics Controller Chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[23:0] bits are display RAM data or command parameters. When D/C='0', D[23:0] bits are commands.

The 8080-series bi-directional interface can be used for communication between the micro controller and LCD driver chip. Interface bus width can be selected with IM3,IM2, IM1 and IM0.

The interface functions of 80-series parallel interface are given in ***Table 5.1.2.***

Table 5.1.2 Parallel interface function (80-Series)

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	0	0	0	8-bit Parallel	0	1	↑	Write 16-bit command, D[7:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[7:0]
					1	↑	1	Read 16/18/24-bit display data, D[7:0]
					1	↑	1	Read 16-bit parameter or status, D[7:0]
0	0	0	1	16-bit Parallel	0	1	↑	Write 16-bit command, D[7:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[15:0]
					1	↑	1	Read 16/18/24-bit display data, D[15:0]
					1	↑	1	Read 16-bit parameter or status, D[15:0]
0	0	1	0	24-bit Parallel	0	1	↑	Write 16-bit command, D[23:0]
					1	1	↑	Write 16/18/24-bit display data or 16-bit parameter, D[23:0]
					1	↑	1	Read 16/18/24-bit display data, D[23:0]
					1	↑	1	Read 16-bit parameter or status, D[23:0]

5.1.2.1 WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[23:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data ('1').

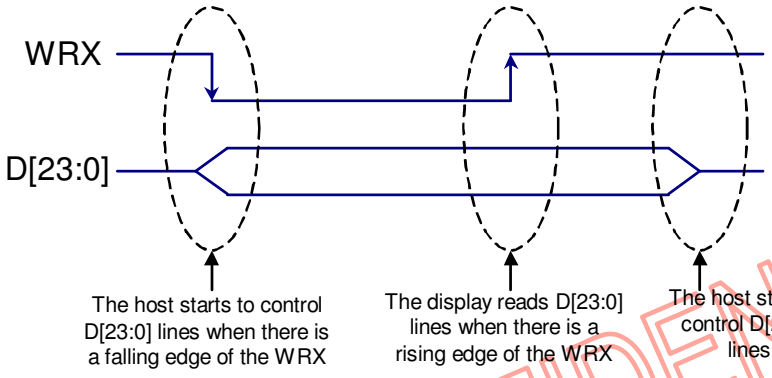


Fig. 5.1.1 80-Series WRX protocol

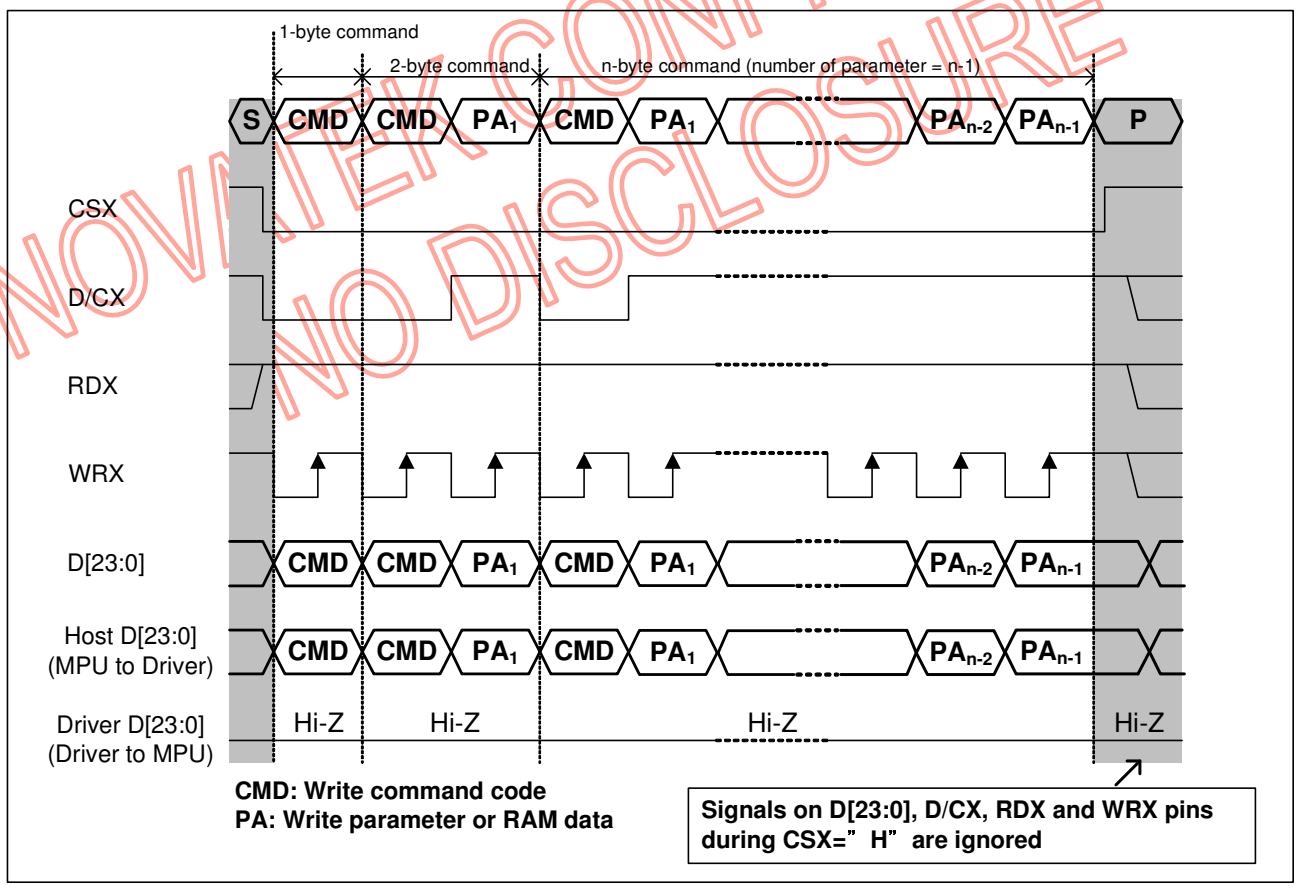


Fig. 5.1.2 80-Series parallel bus protocol, write to register or display RAM

5.1.2.2 READ CYCLE SEQUENCE

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

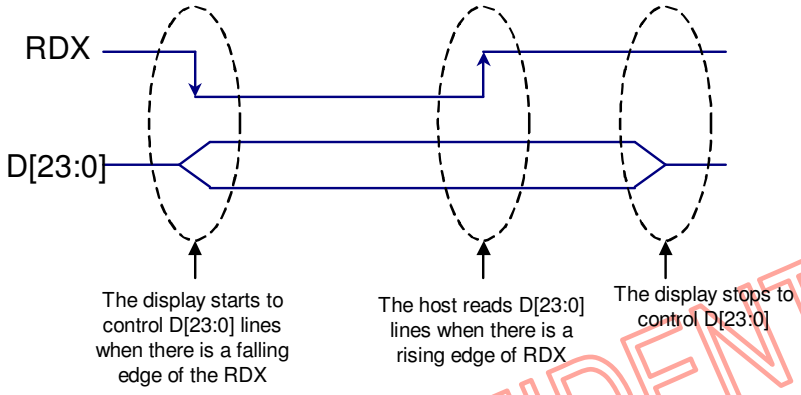


Fig. 5.1.3 80-Series RDX protocol

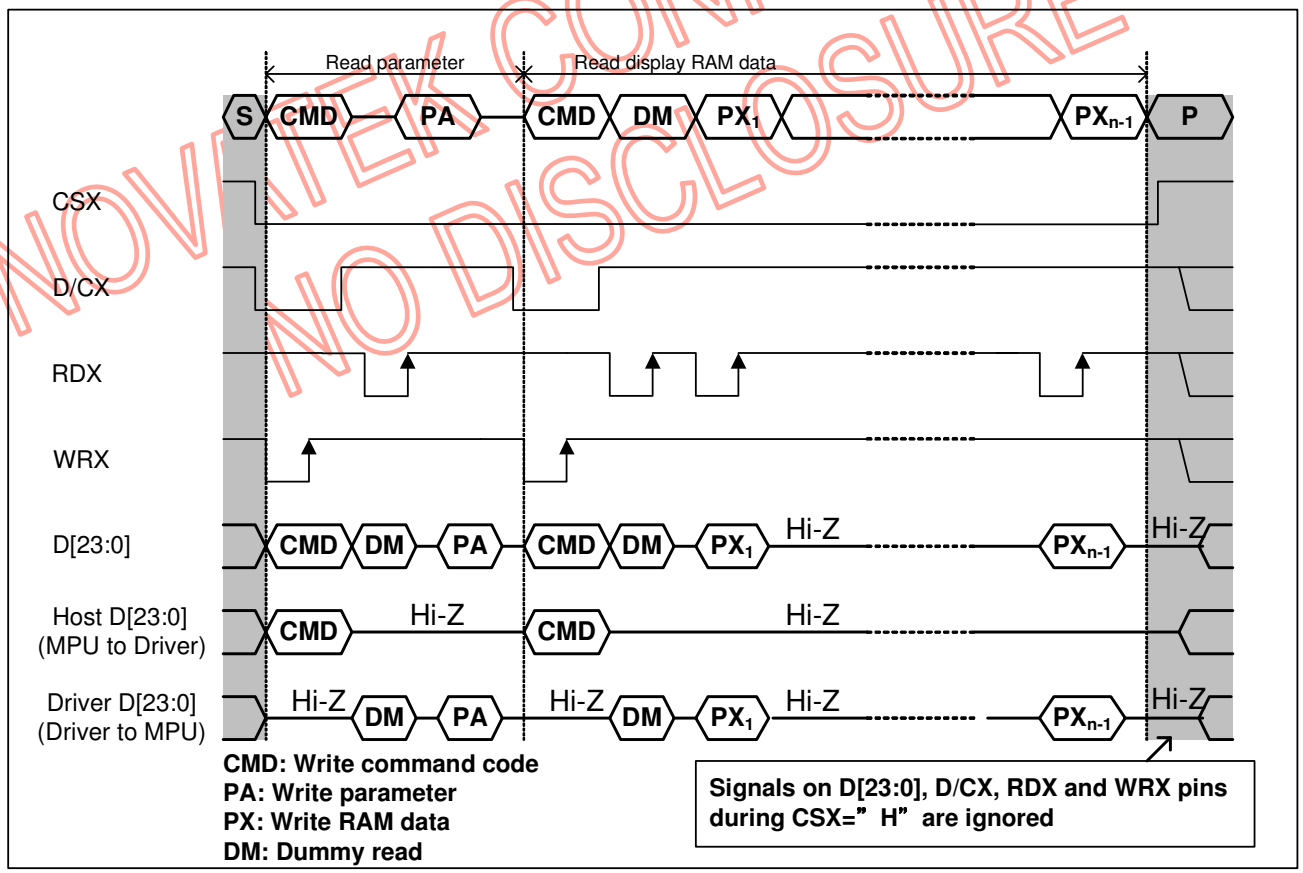


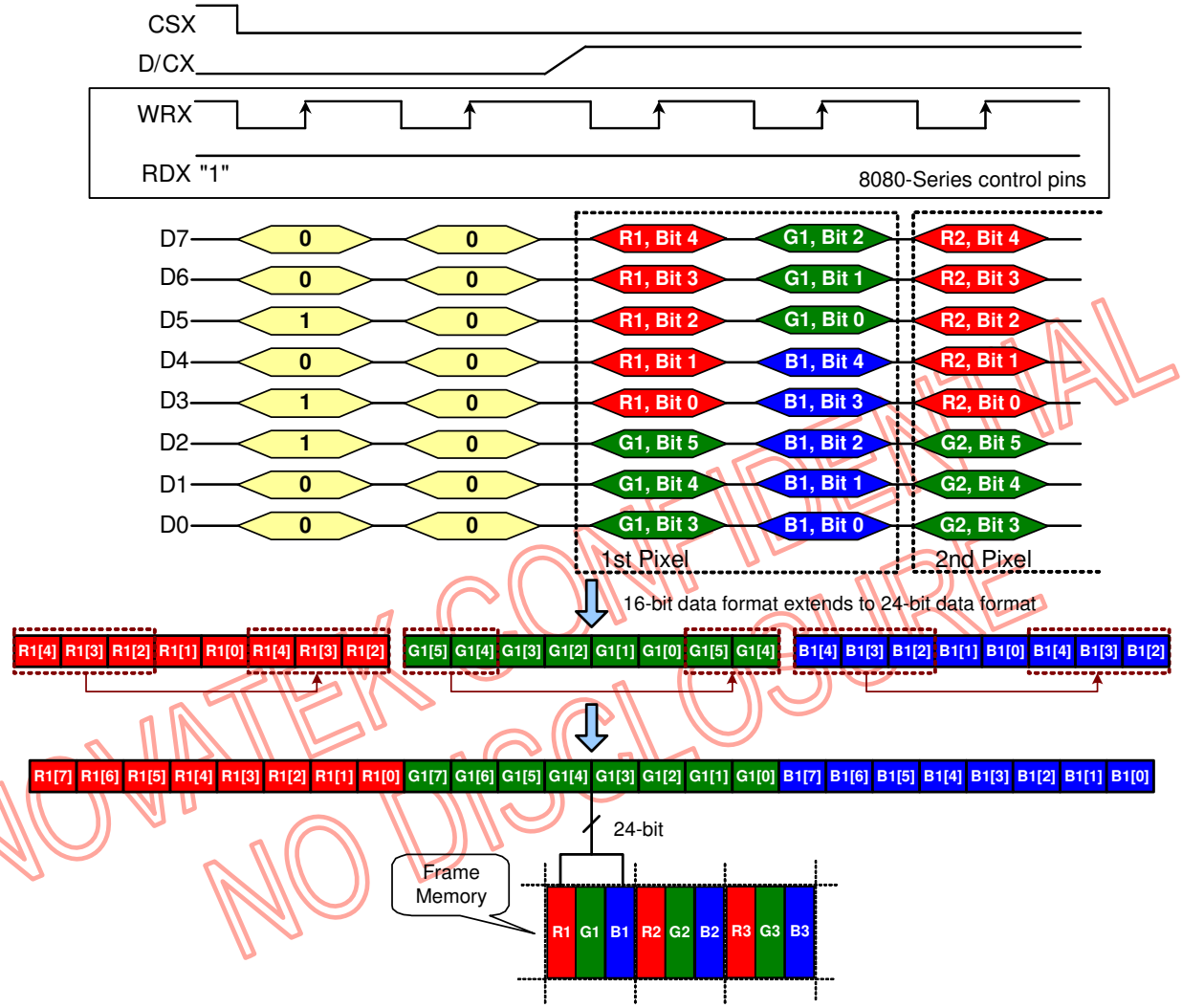
Fig. 5.1.4 80-Series parallel bus protocol, read from register or display RAM

5.1.2.3 8-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	2Ch
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	B4	B3	B2	B1	B0	
0006h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	
0007h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	

- 65K colors, RGB is 5-6-5-bit pixel data input



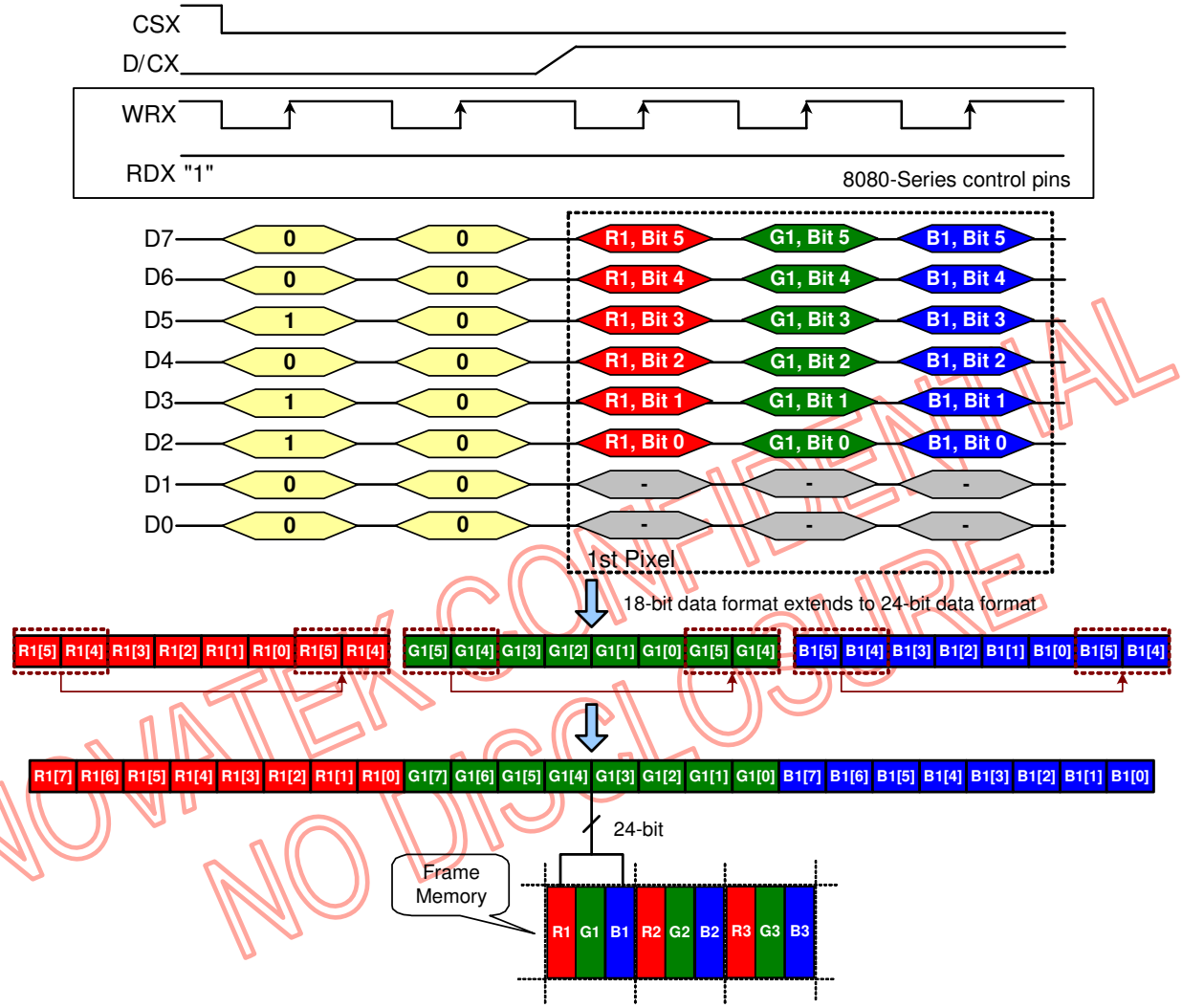
NOTES:

1. 2 times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bit pixel data input



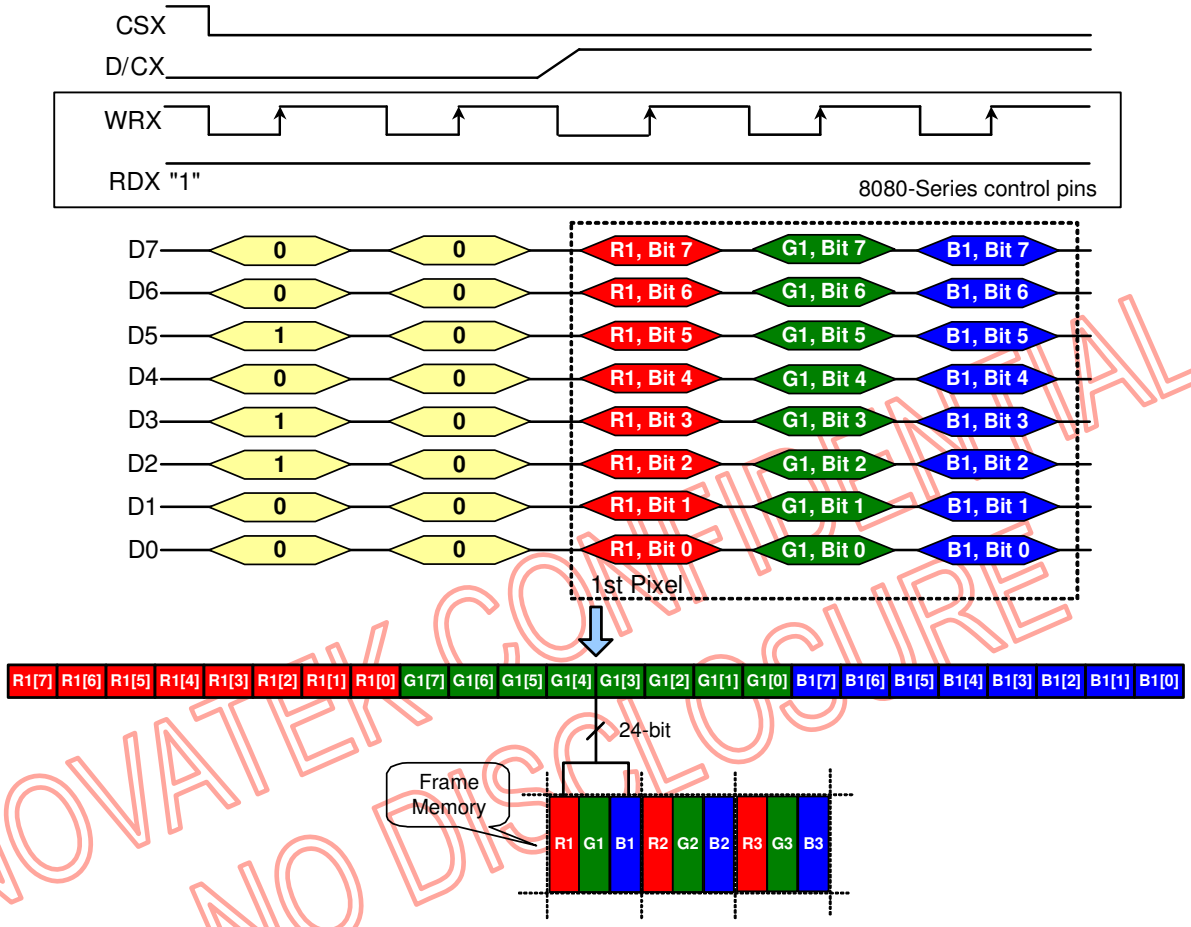
NOTES:

1. 3 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



NOTES:

1. 3 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.

2. The most significant bits are Rx7, Gx7 and Bx7.

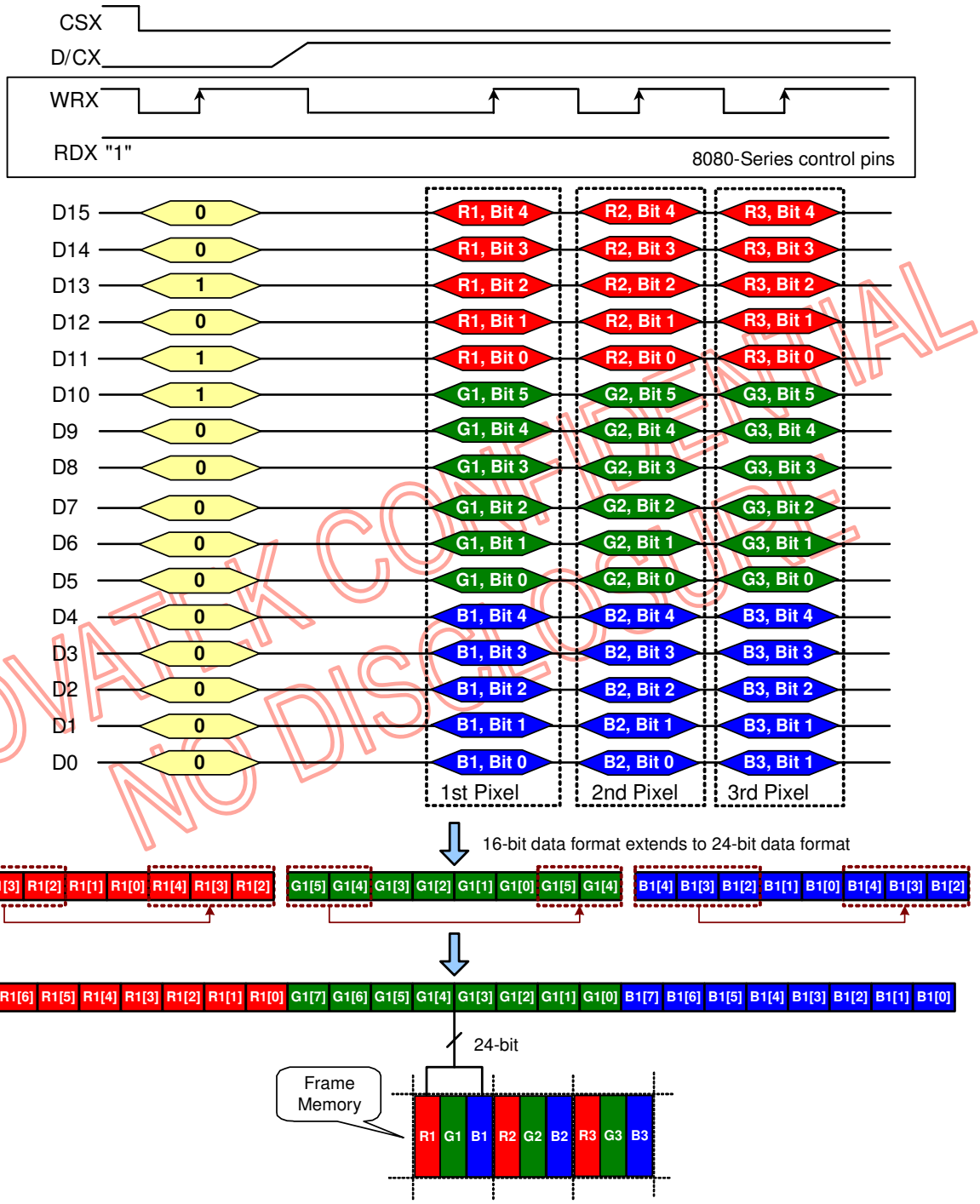
3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.4 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
0006h	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color
	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	
0007h	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0	
	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	

- 65K colors, RGB is 5-6-5-bit pixel data input

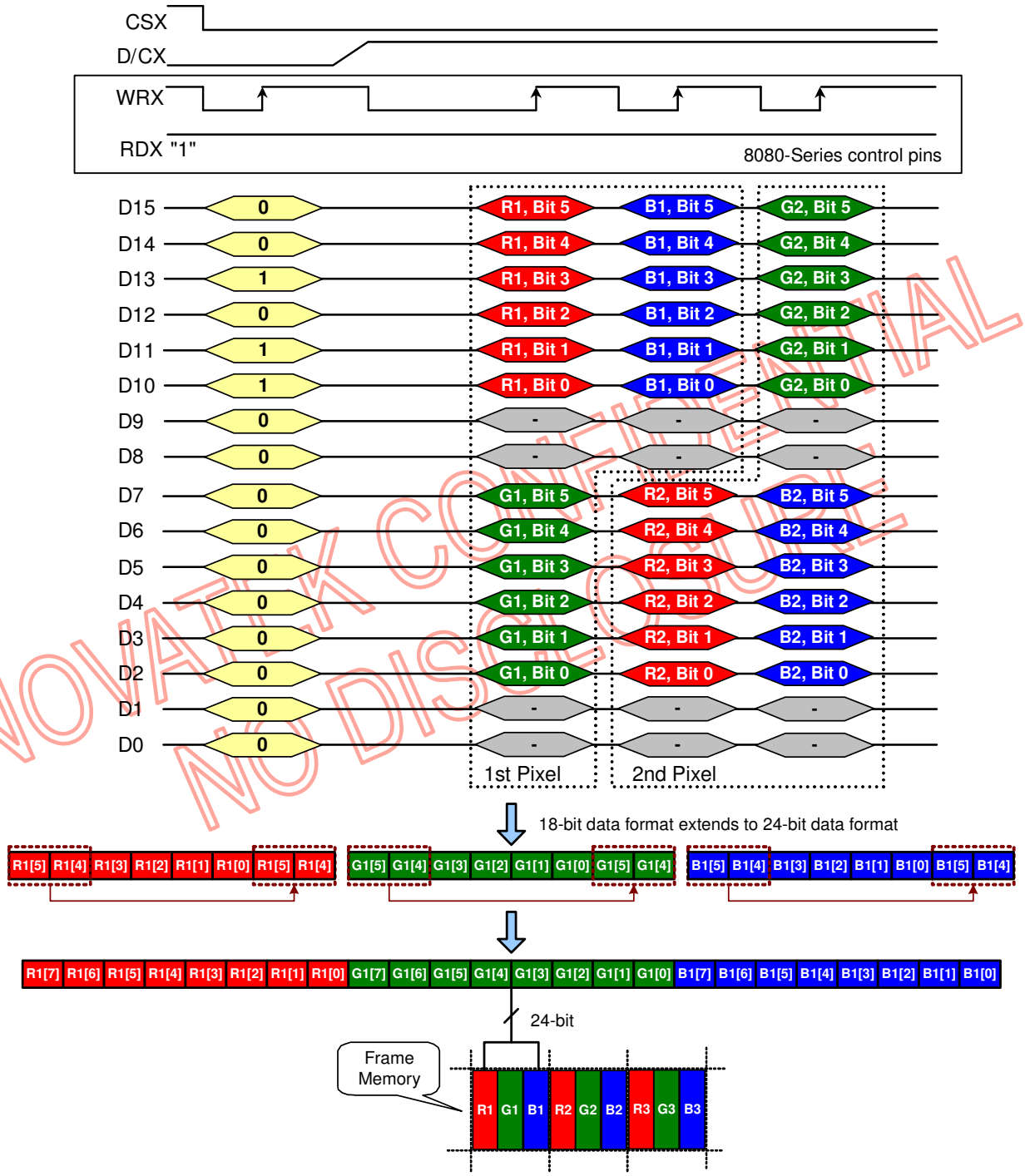


1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bit pixel data input

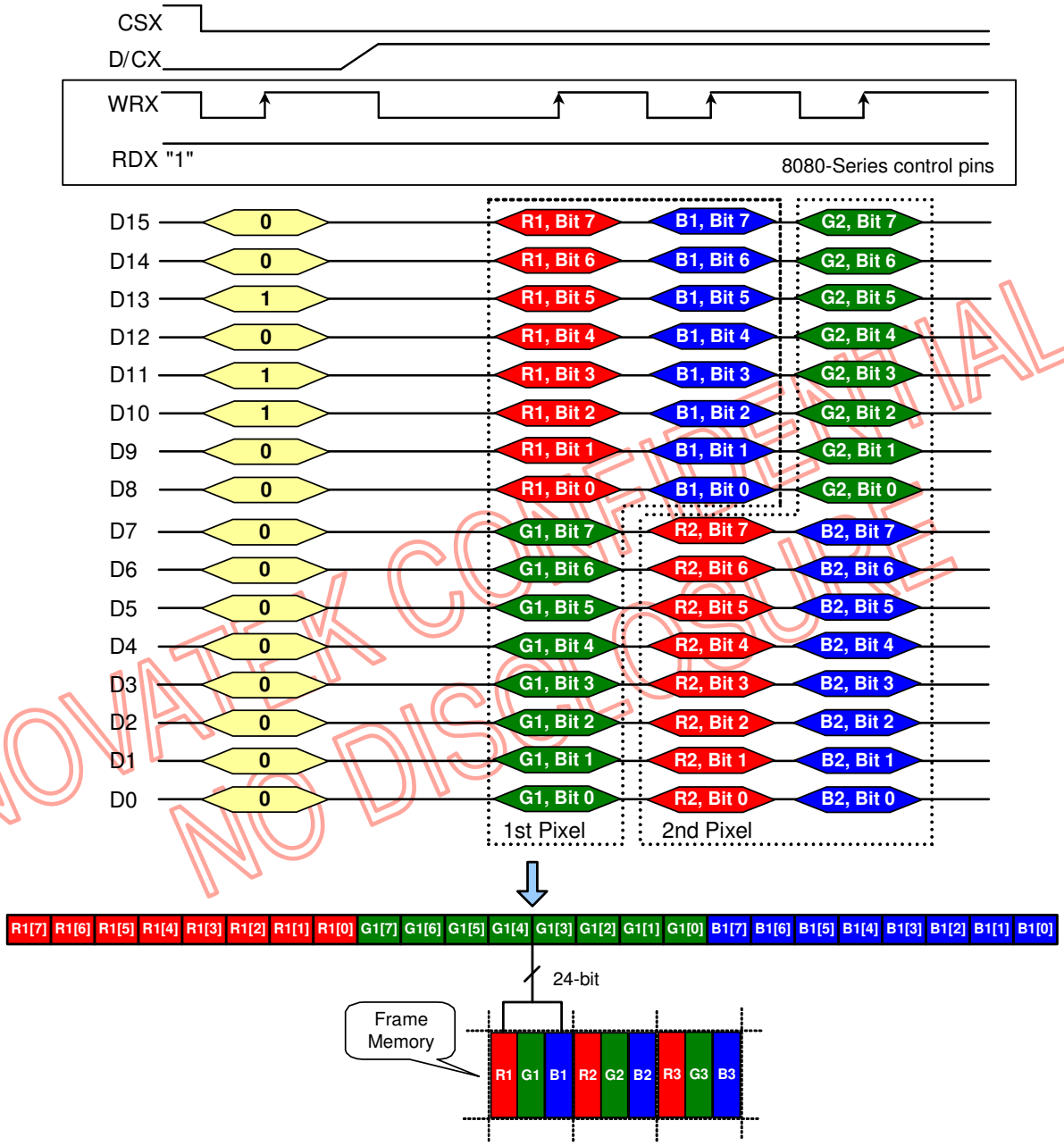


1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



1. 3 times transfer is used to transmit 2 pixel data or 2 times transfer is used to transmit 1 pixel data with the 24-bit color depth information.

2. The most significant bits are Rx7, Gx7 and Bx7.

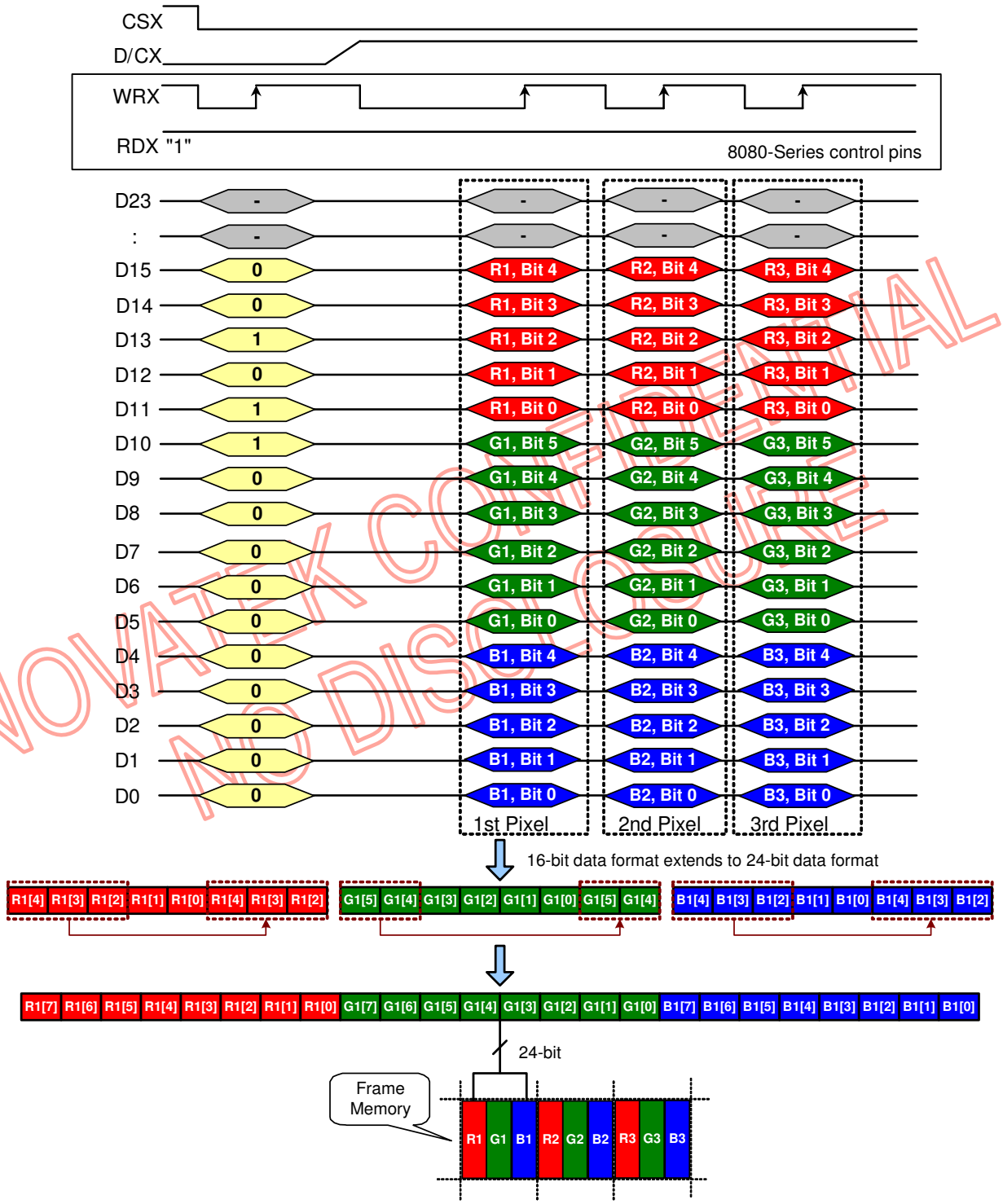
3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.5 24-BIT PARALLEL INTERFACE FOR DATA RAM WRITE

Different display data formats are available for three color depths supported by the LCM listed below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	2C00h
3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
0005h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	65K-Color
0006h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color
0007h								R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color

- 65K colors, RGB is 5-6-5-bit pixel data input

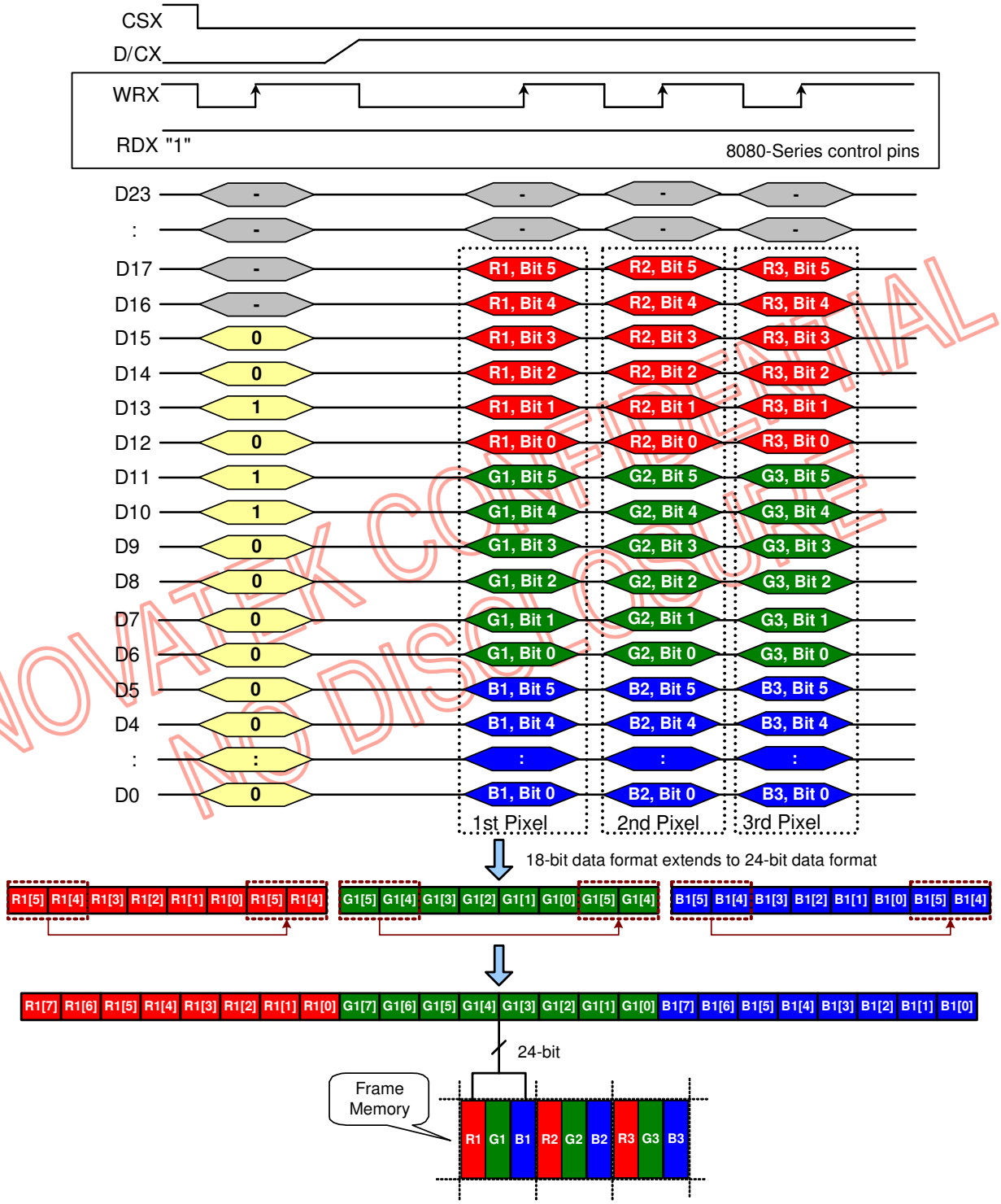


1. In one transfer (D15 to D0), 1 pixel data transmitted with the 16-bit color depth information.

2. The most significant bits are Rx4, Gx5 and Bx4.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 262K colors, RGB is 6-6-6-bi pixel data t input

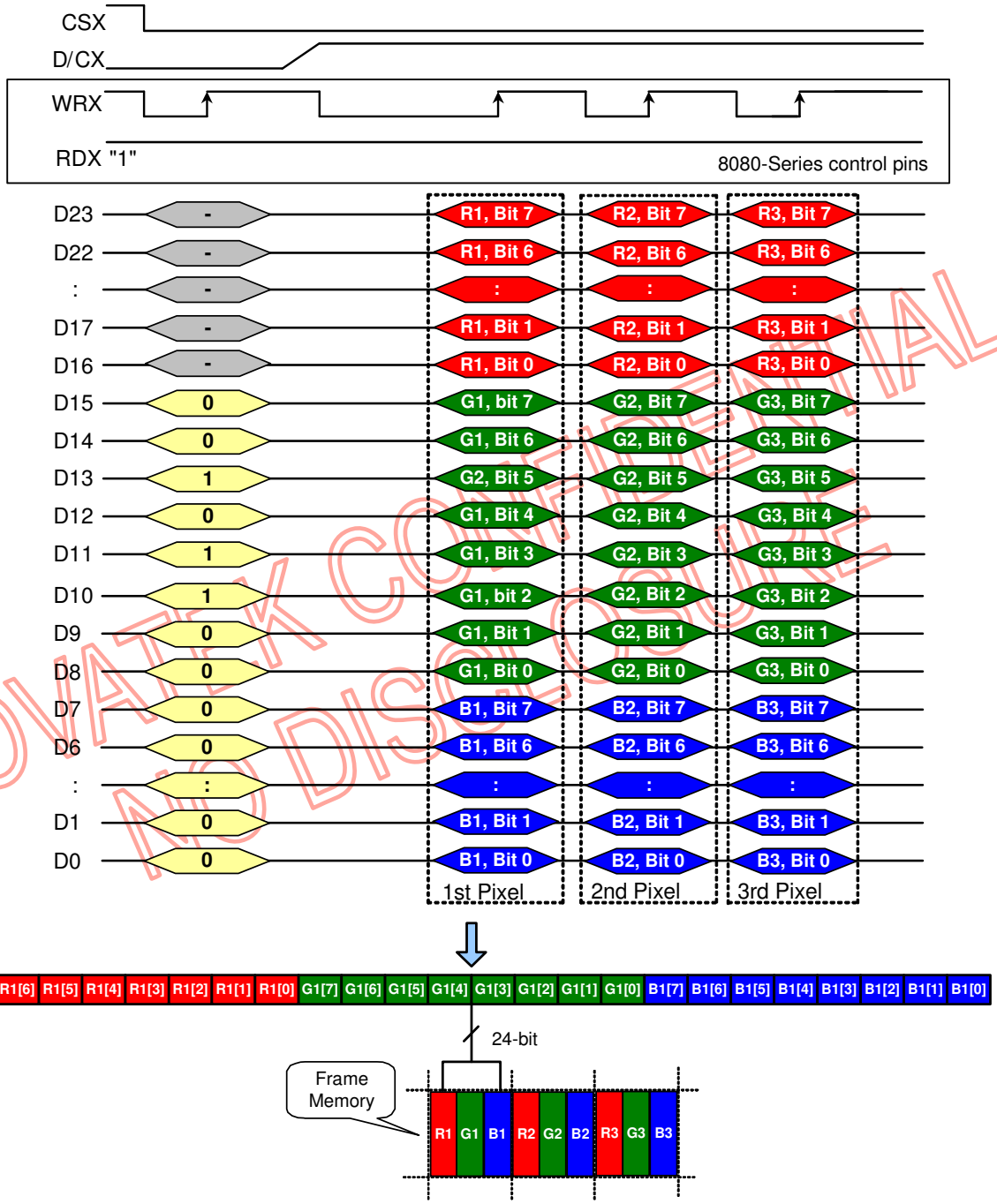


1. In one transfer (D17 to D0), 1 pixel data transmitted with the 18-bit color depth information.

2. The most significant bits are Rx5, Gx5 and Bx5.

3. The least significant bits are Rx0, Gx0 and Bx0.

- 16M colors, RGB is 8-8-8-bit pixel data input



1. In one transfer (D23 to D0), 1 pixel data transmitted with the 24-bit color depth information.

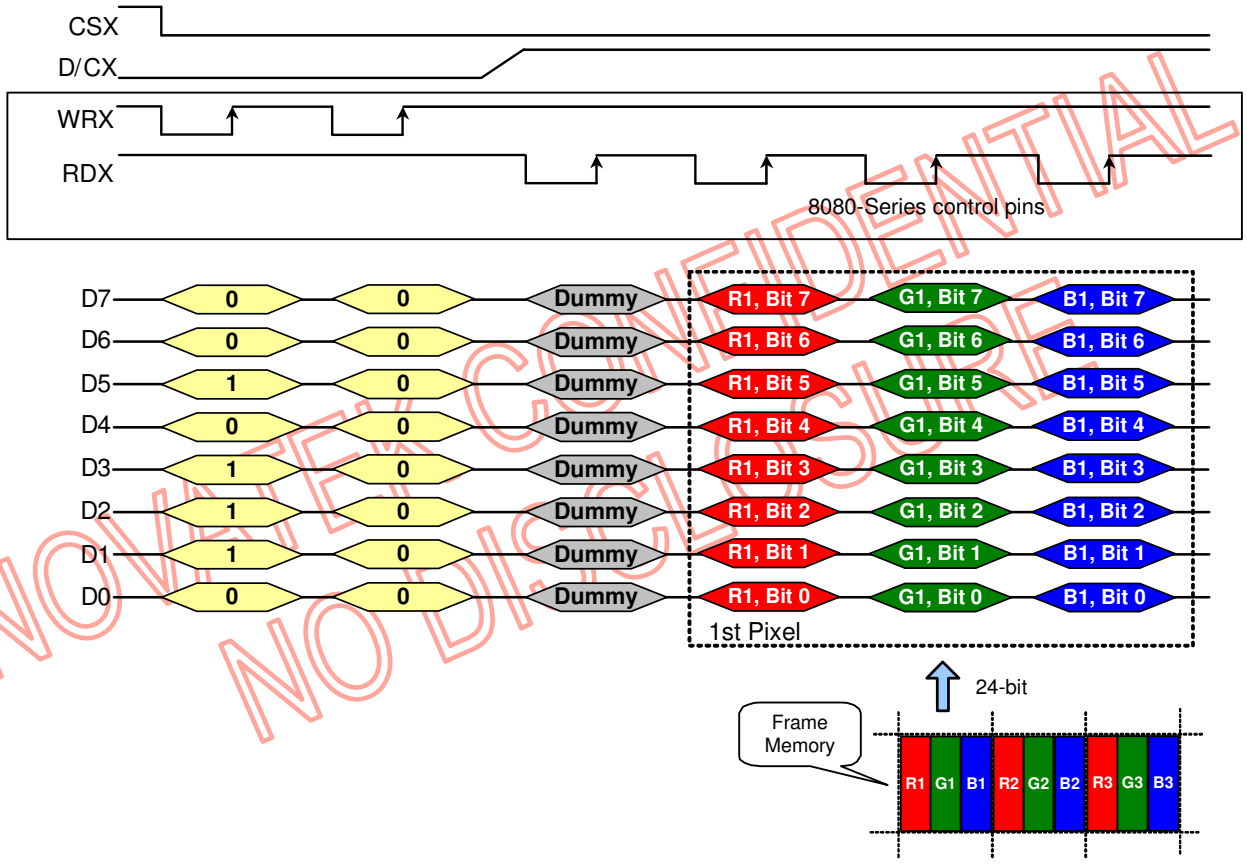
2. The most significant bits are Rx7, Gx7 and Bx7.

3. The least significant bits are Rx0, Gx0 and Bx0.

5.1.2.6 8-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

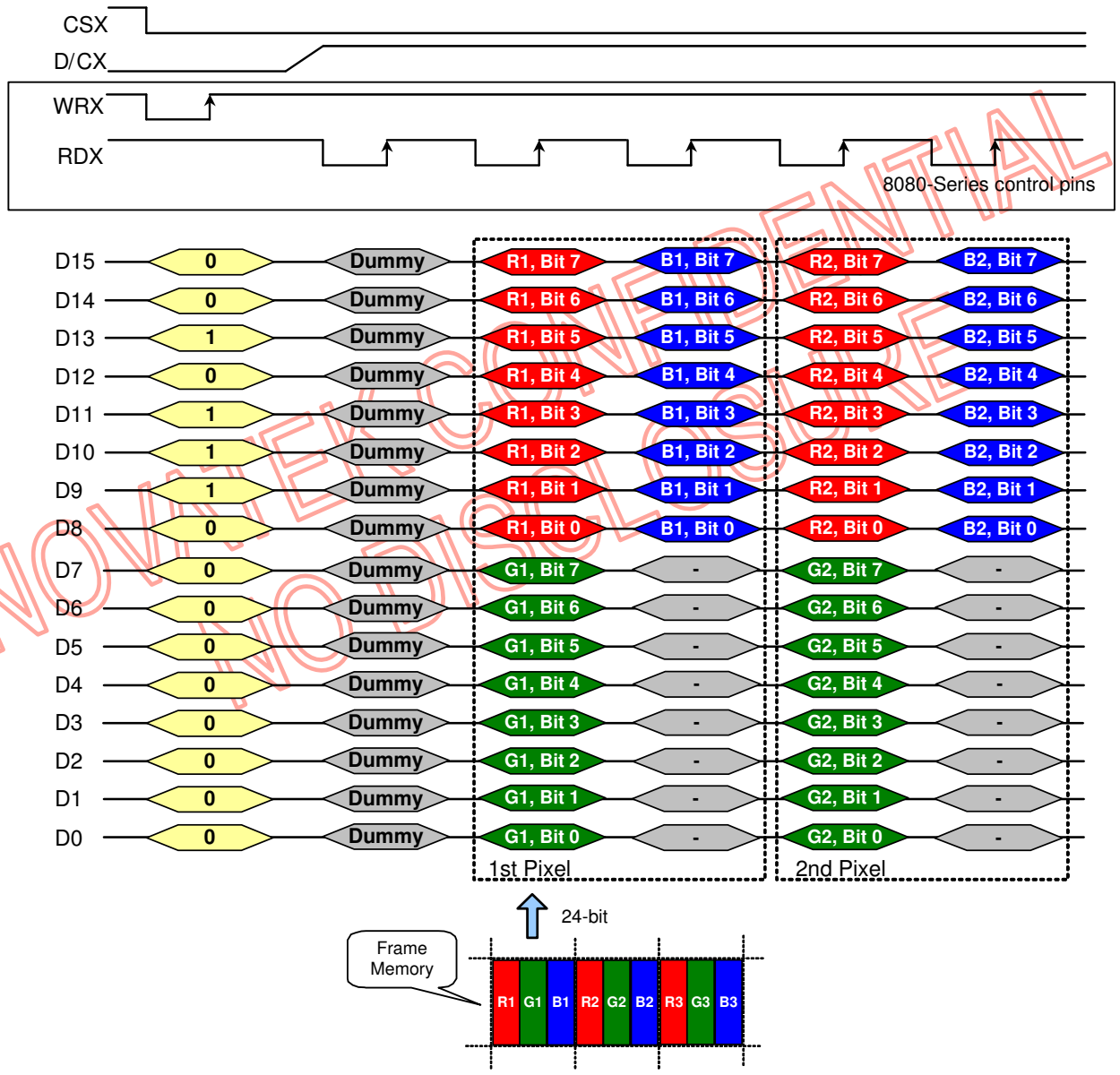
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
Register Command	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	2Eh
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	00h
	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
Read Data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	16.7M-Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	G7	G6	G5	G4	G3	G2	G1	G0	
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	



5.1.2.7 16-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

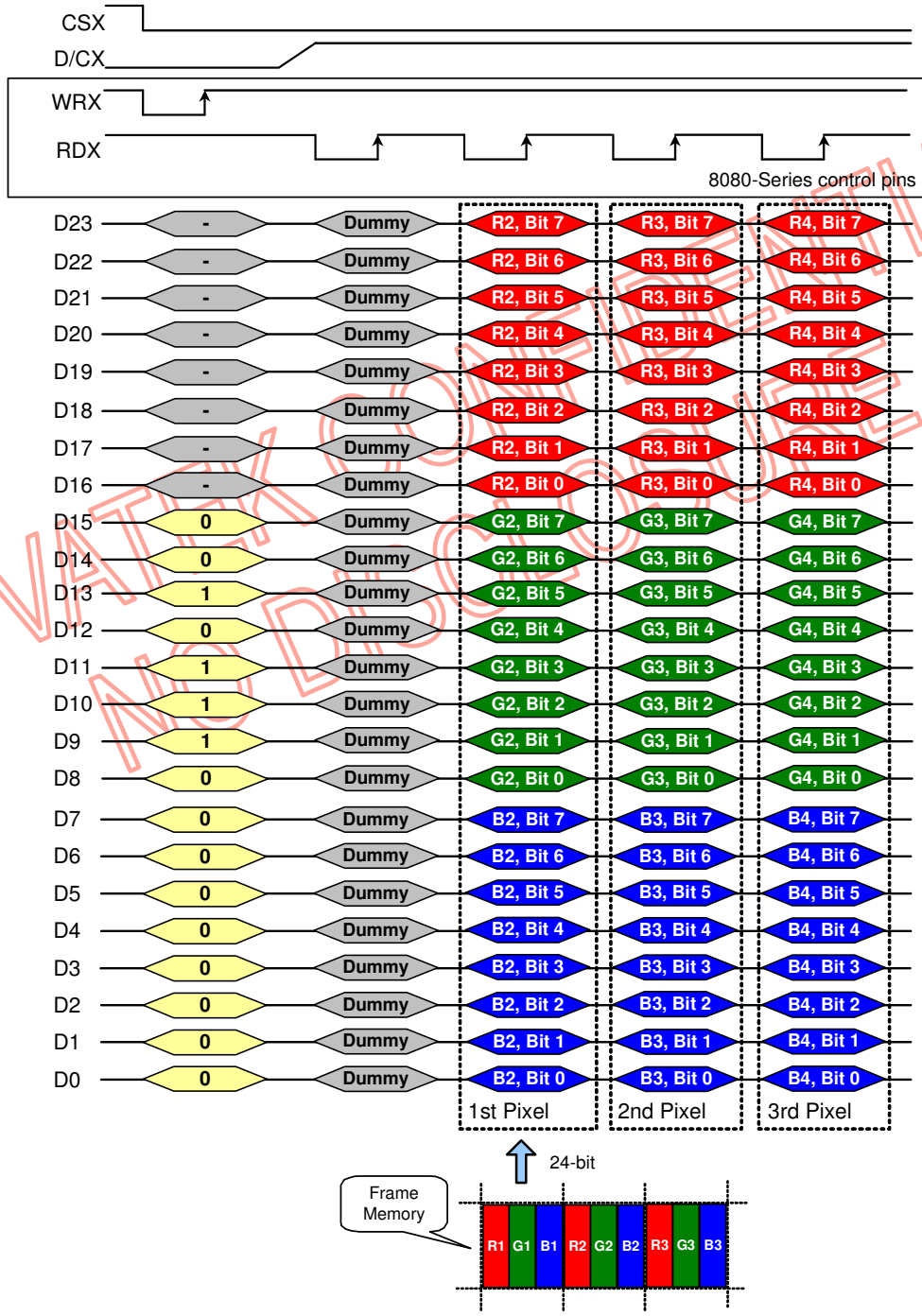
Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read Data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	16.7M-Color
	x	x	x	x	x	x	x	x	B7	B6	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	



5.1.2.8 24-BIT PARALLEL INTERFACE FOR DATA RAM READ

The read data for RGB is 8-8-8-bit output as below.

Register Command	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	2E00h
Read Data	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
								R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	16.7M-Color



5.1.3 Serial Interface

The selection of this interface is done by IM3, IM2, IM1 and IM0.

The serial interface can select IM3 = 0 or 1 to decide the trigger edge of serial clock (SCL) is rising edge or falling edge. The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

5.1.3.1 WRITE MODE

The write mode of the interface means the micro controller writes commands and data to the NT35510. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low (see ***Fig. 5.1.5***). SDI/SDO are sampled at the rising edge of SCL. R/W indicates, whether the byte is read command (R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

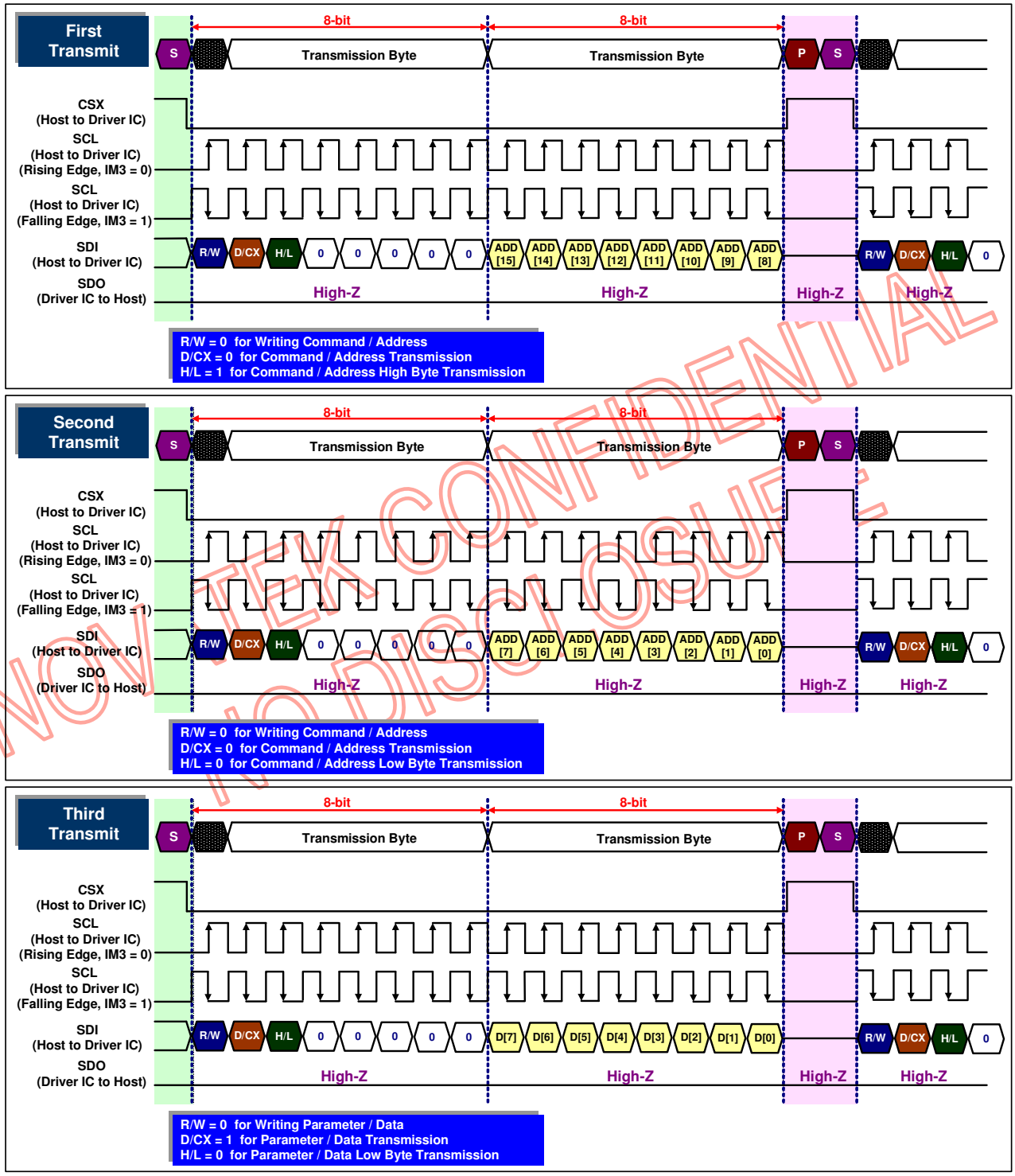


Fig. 5.1.5 Serial bus protocol for register write mode

5.1.3.2 READ MODE

The read mode of the interface means that the micro controller reads register value from the NT35510. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send (see ***Fig. 5.1.6***). The NT35510 samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges. Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (16 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

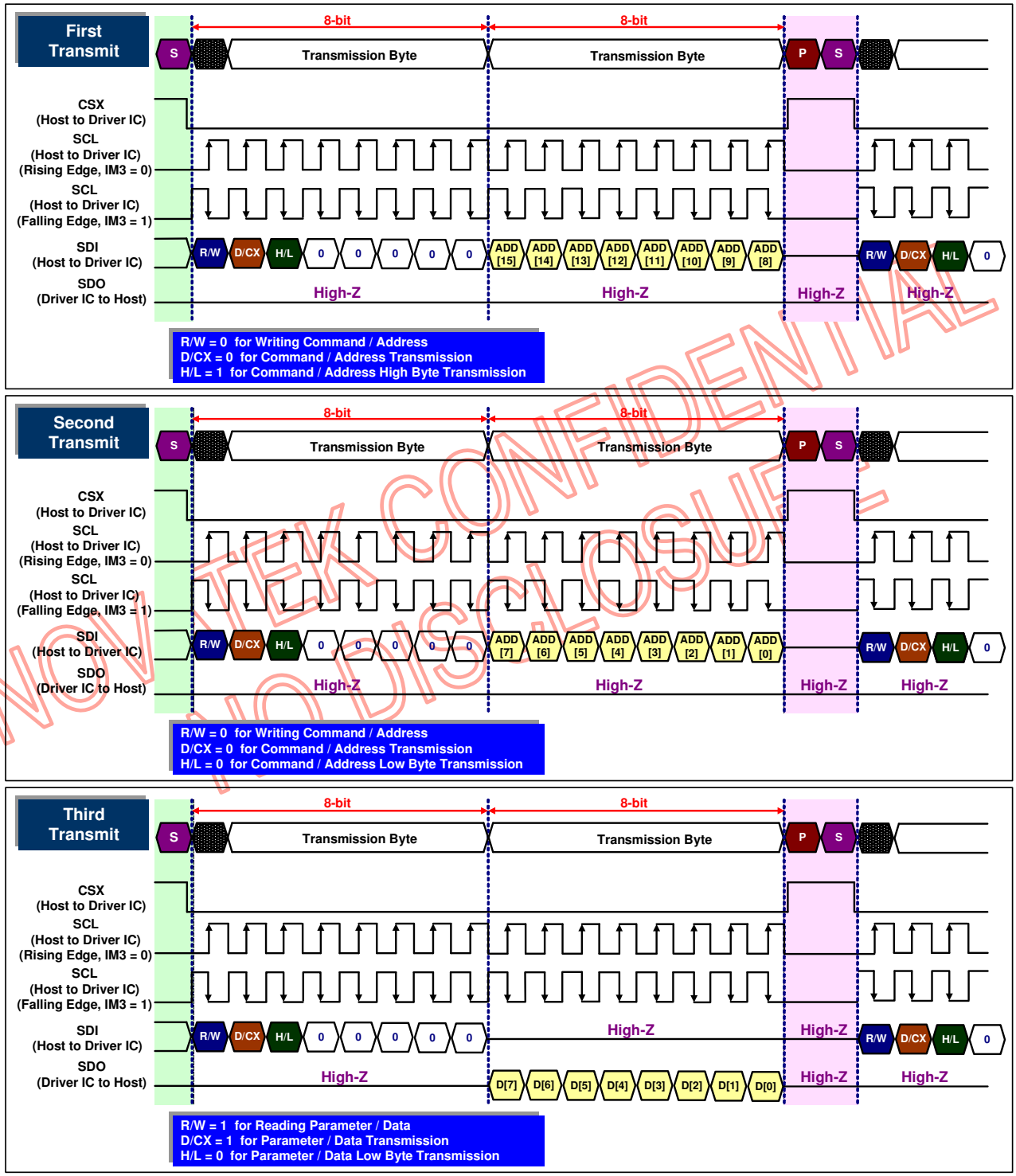
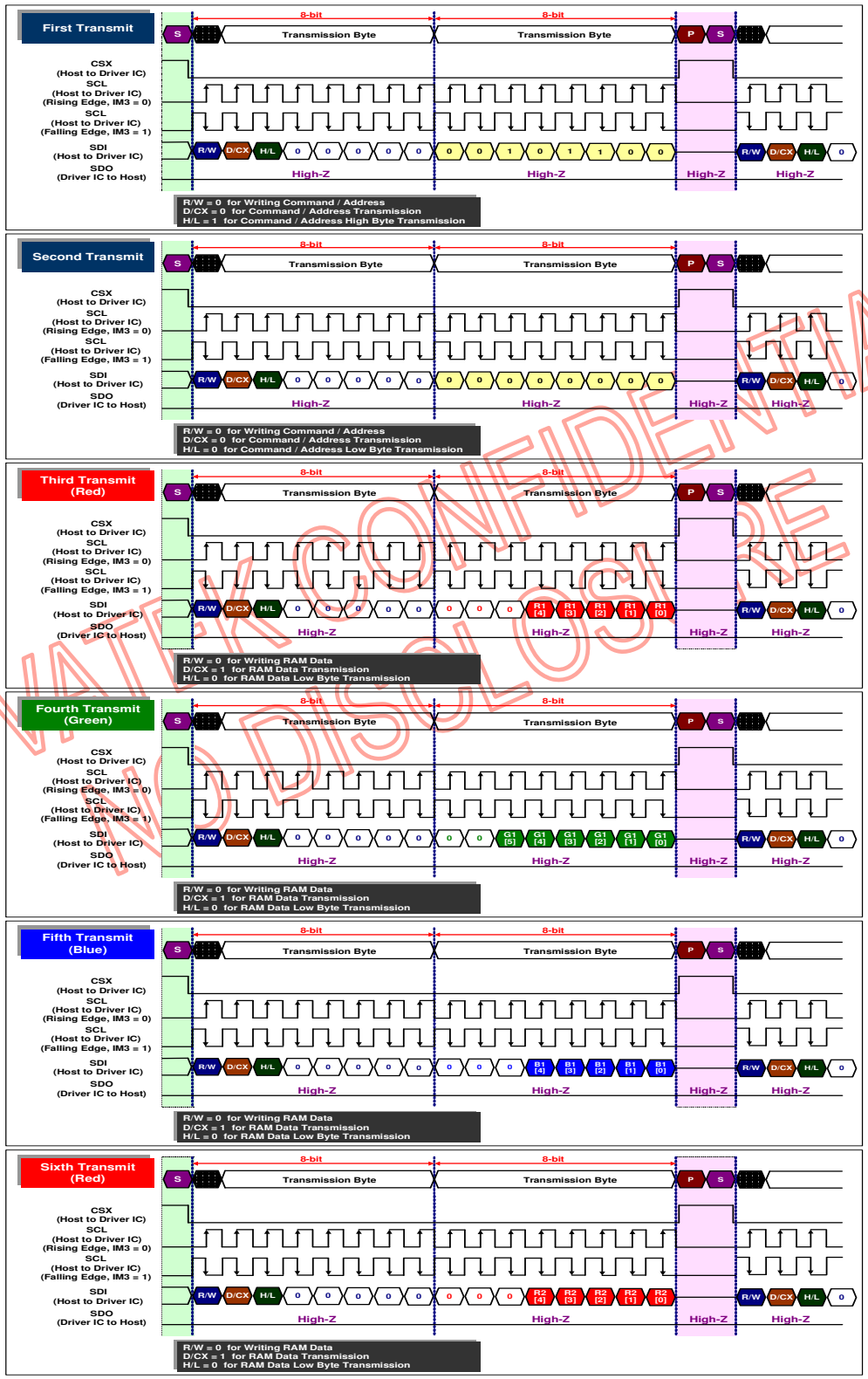


Fig. 5.1.6 Serial bus protocol for register read mode

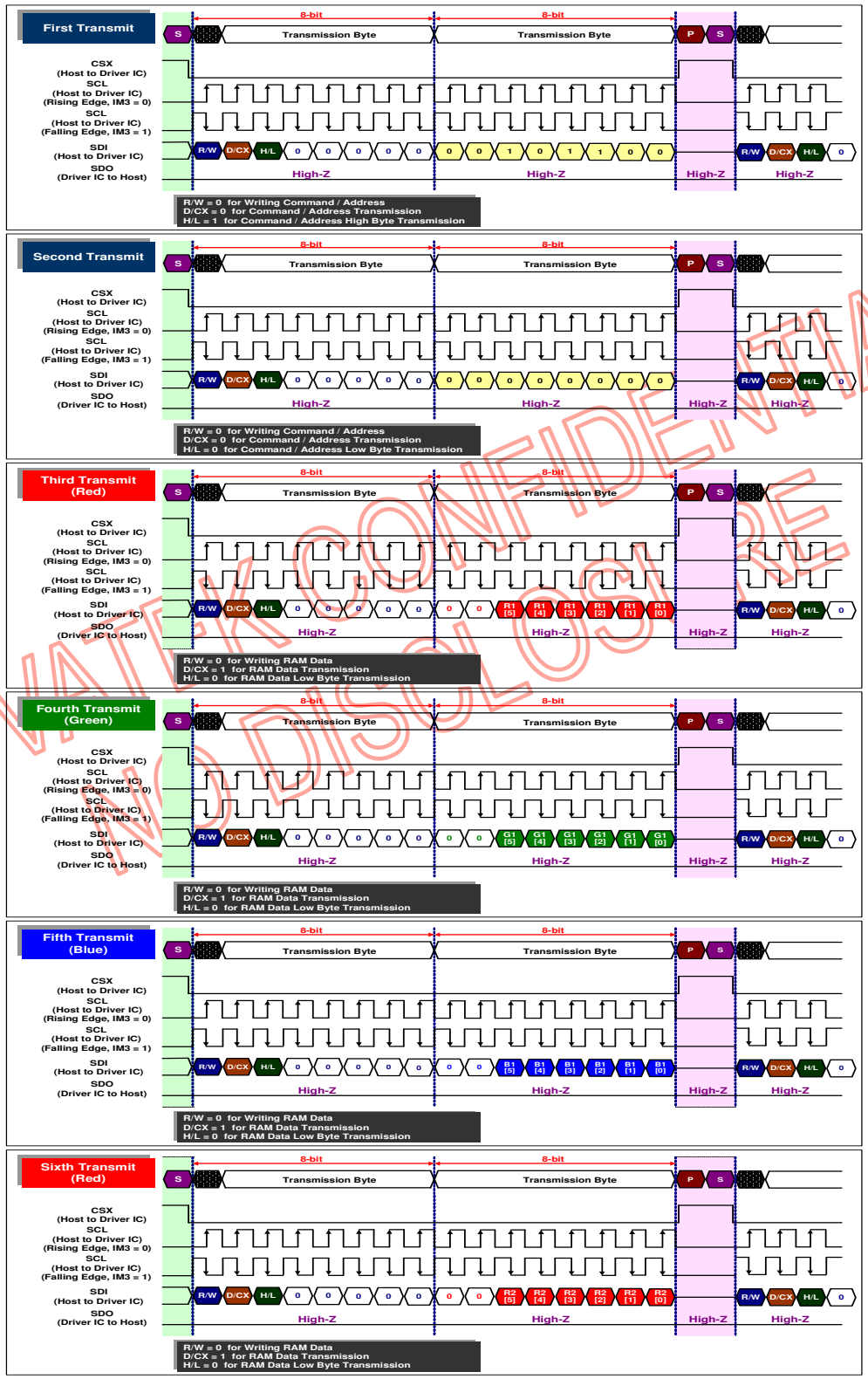
5.1.3.3 SERIAL INTERFACE FOR DATA RAM WRITE

The serial interface is used with RGB interface (IM[2:0]=”011”) or MDDI interface (IM[2:0]=”110”). In RGB+SPI interface, the data RAM write function for SPI is valid when bit ICM=”1” (command B300h of page 0). In MDDI+SPI interface, the data RAM write function for SPI is valid when MDDI is not writing data to RAM. Different display data formats are available for three color depths supported by the LCM listed below:

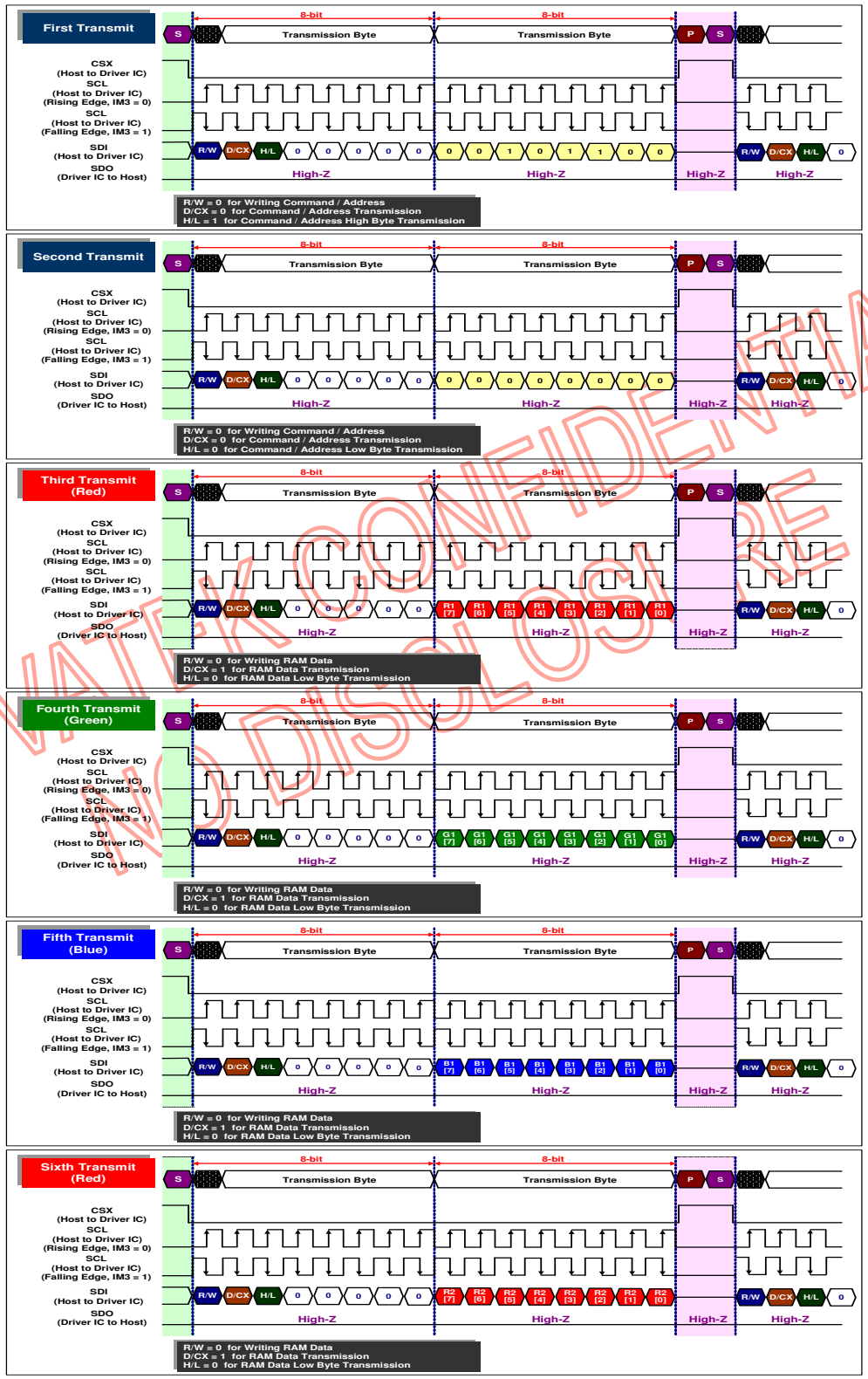
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)



- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006)

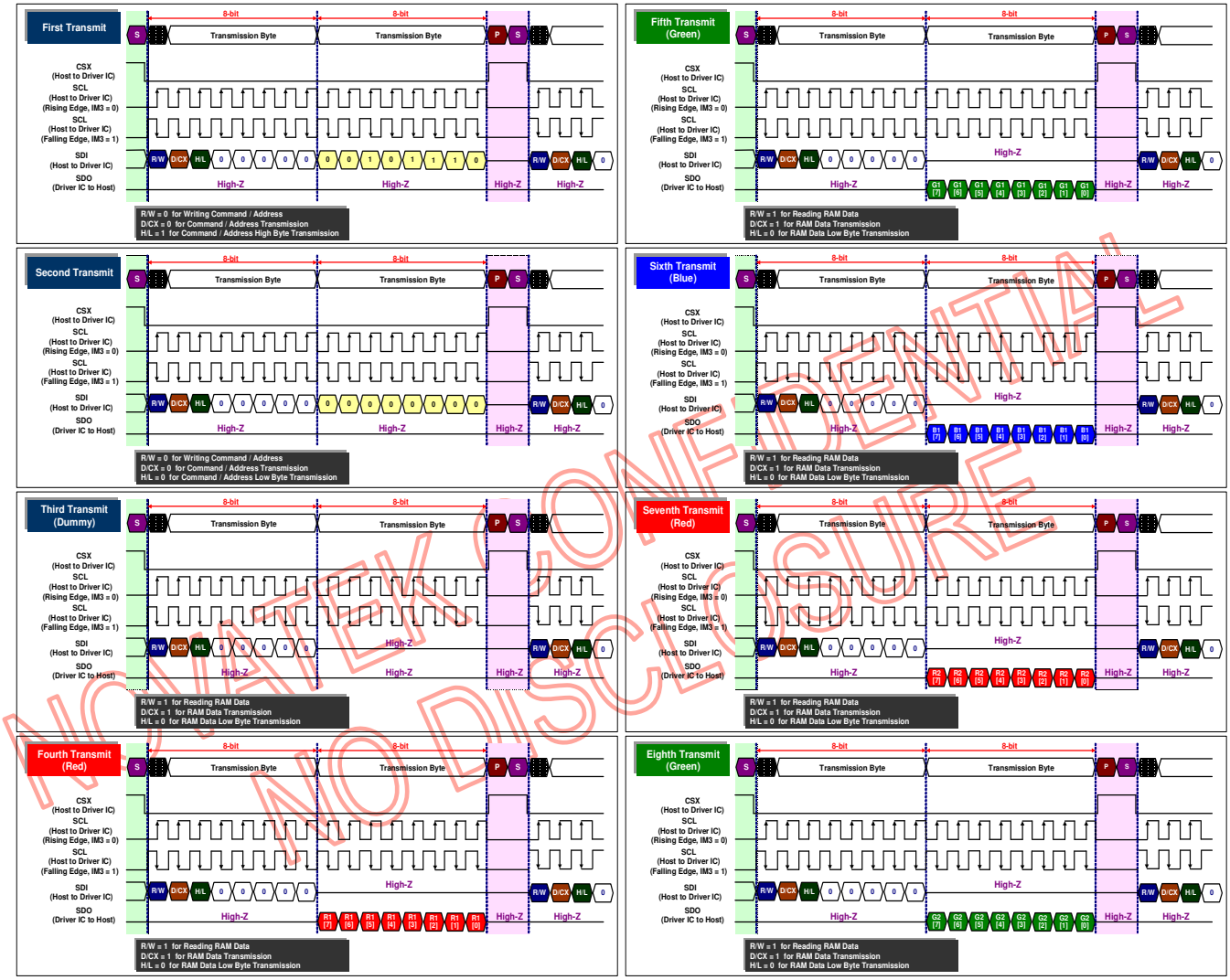


- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)



5.1.3.4 SERIAL INTERFACE FOR DATA RAM READ

The read data RGB is 8-8-8-bit output as below.



5.2 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data line (I2C_SDA) and the Serial Clock Line (I2C_SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledgement related clock pulse. A slave receiver which is addressed must generate an acknowledgement after the reception of each byte. Also a master receiver must generate an acknowledgement after the reception of each byte that has been clocked out of the slave transmitter.

(a) I2C-Bus Protocol:
Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. There are four slave address can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

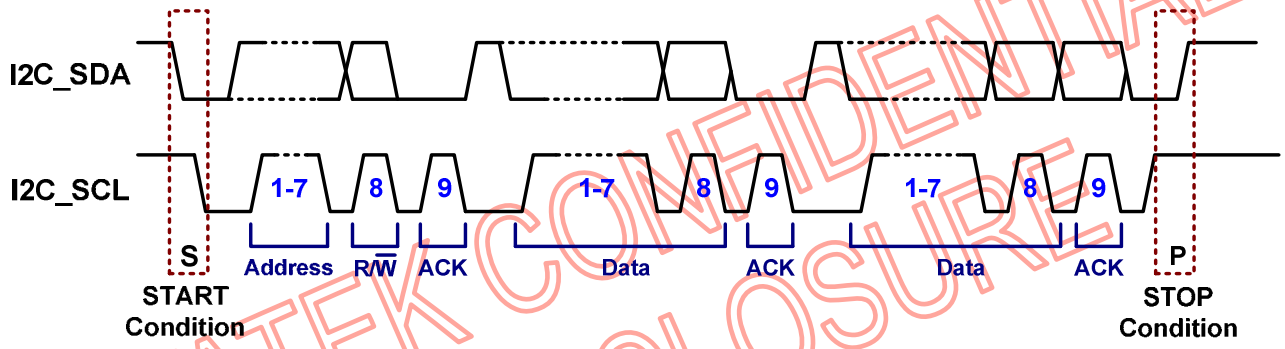


Fig. 5.2.1 Definition of I2C-Bus Protocol

(b) Definitions:
- Transmitter: The device which sends the data to the bus.
- Receiver: The device which receives the data from the bus.
- Master: The device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

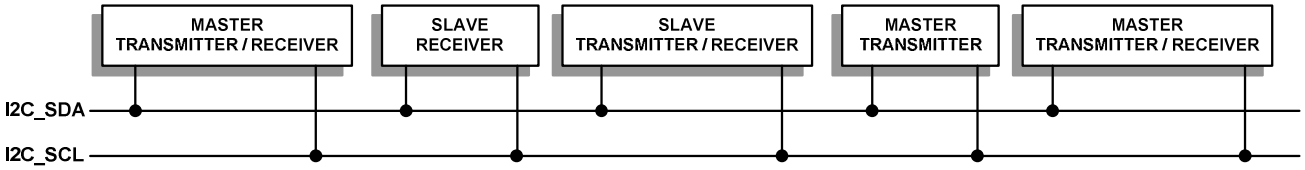


Fig. 5.2.2 System Configuration

5.2.1 Slave Address of I2C

NT35510 supports two slave addresses, 1001100, 1001101 after the START procedure via I2C bus for MCU usage .There are 1 hard pin, I2C_SA0 to determine the difference slave address. The slave address selection is described as the following table. The I2C interface address is selected from the external MPU.

Table 5.2.1 Selection Table of Slave Address

I2C_SA0	Slave Address	Notes
0	1001100	0000xxx and 1111xxx: Reversed
1	1001101	

5.2.2 Register Write Sequence of I2C Interface

NT35510 supports register write sequence via I2C-bus transfer. The detail transference sequences are illustrated and described as below.

(1) Data transfers for register writing follow the format is shown in Fig.5.2.2.
(2) After the START condition (S), a slave address is sent. R/W bit is setting to "zero" for WRITE.
(3) The slave issues an ACK to master.
(4) 16 bits register high byte address transfer first. Then transfer the register low byte address.
(5) 16 bits register high byte data of parameter transfer first. Then transfer the register low byte data parameter.
(6) A data transfer is always terminated by a STOP condition.

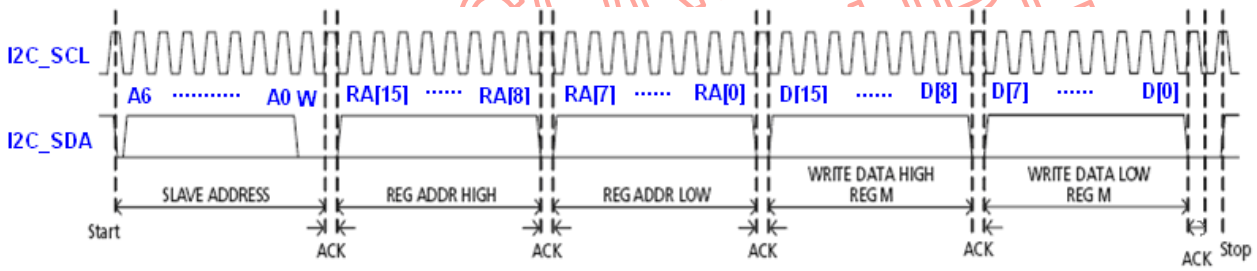


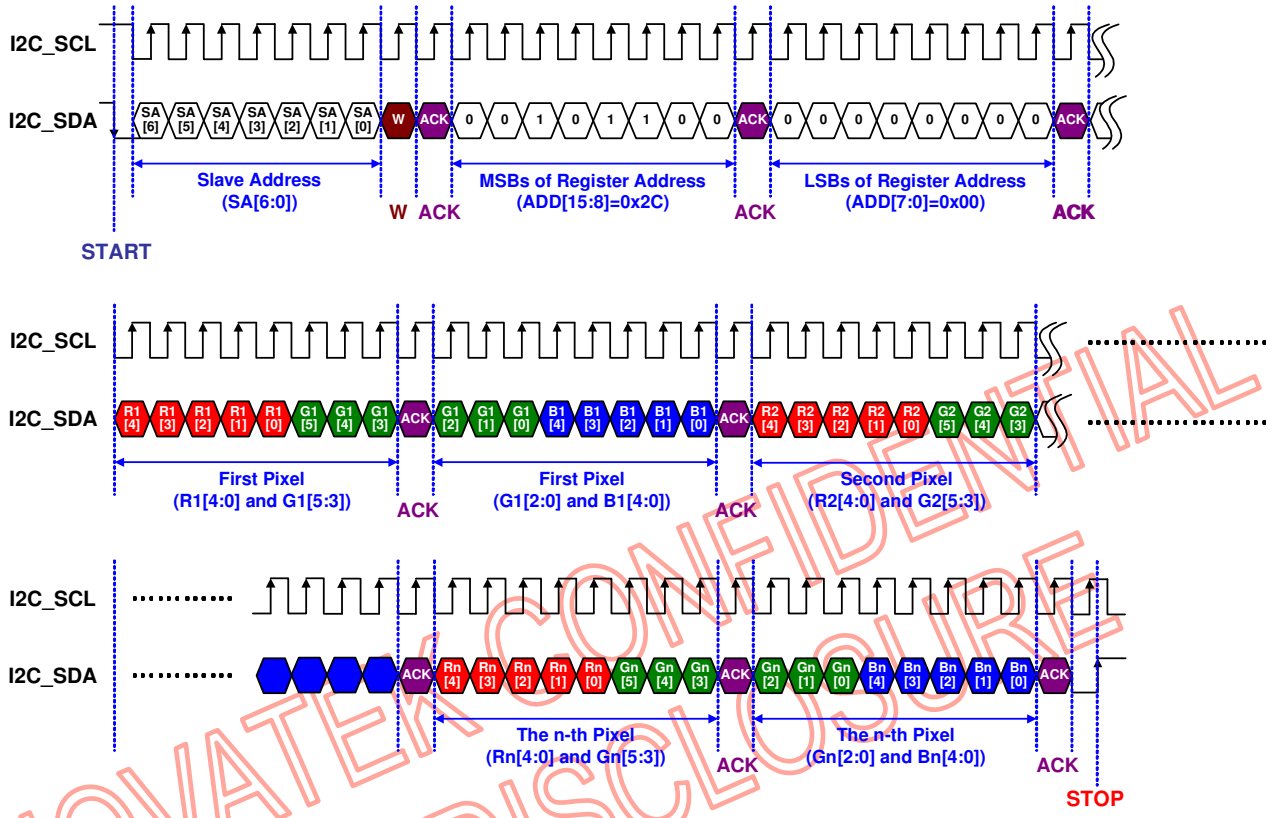
Fig. 5.2.3 Register Writing Timing of I2C Interface

5.2.3 RAM Data Write Sequence of I2C Interface

NT35510 supports sequential RAM data writing via I2C-Bus. NT35510 will increase the RAM address automatic by window address when the Host MCU write the RAM data via this way. The transfer protocol of window address setting can refer to the 5.2.3 Register Write Sequence. Different display data formats are available for three color depths supported by the LCM.

The sequential RAM writing timing is shown in below.

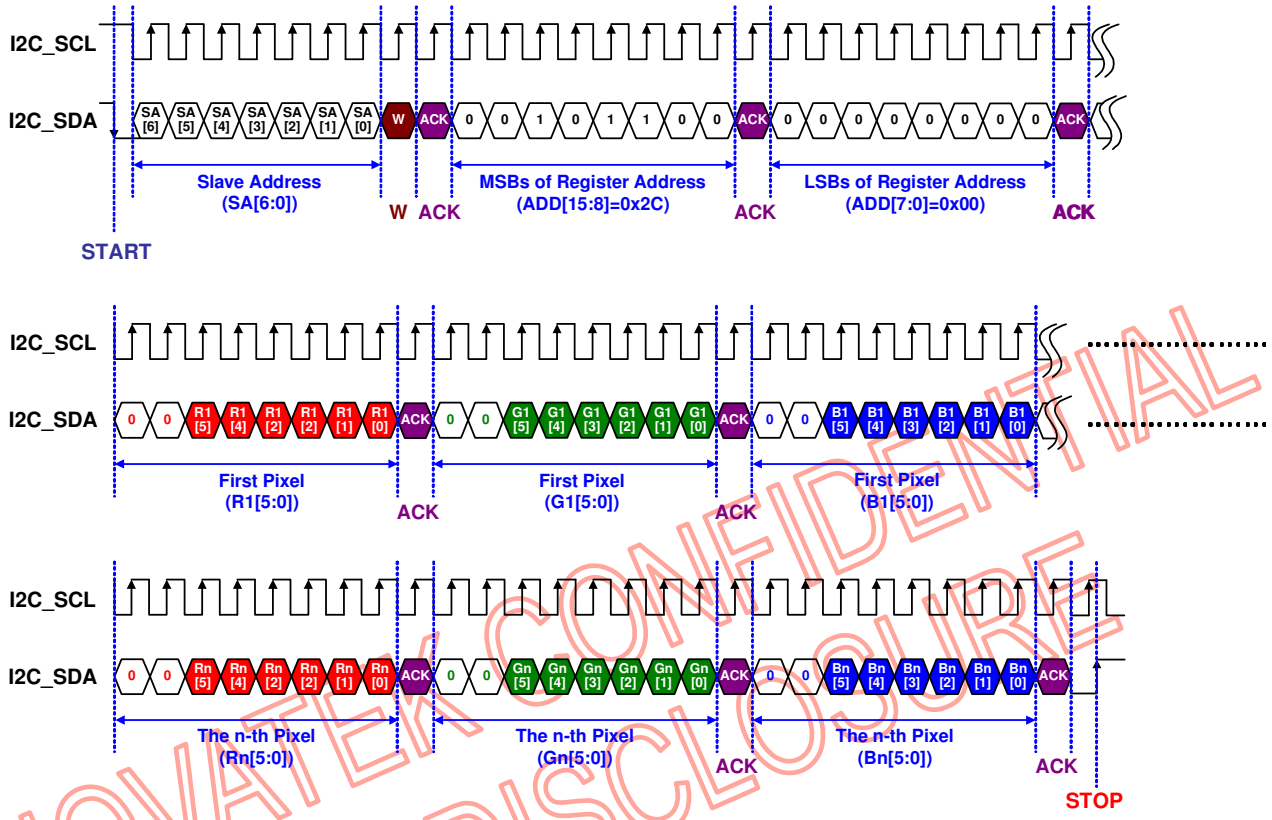
- 65K colors, RGB is 5-6-5-bit pixel data input (parameter of command 3A00h is 0x0005)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[4:0], R2[4:0], ···, Rn[4:0]: The red color data of each pixel
G1[5:0], G2[5:0], ···, Gn[5:0]: The green color data of each pixel
B1[4:0], B2[4:0], ···, Bn[4:0]: The blue color data of each pixel

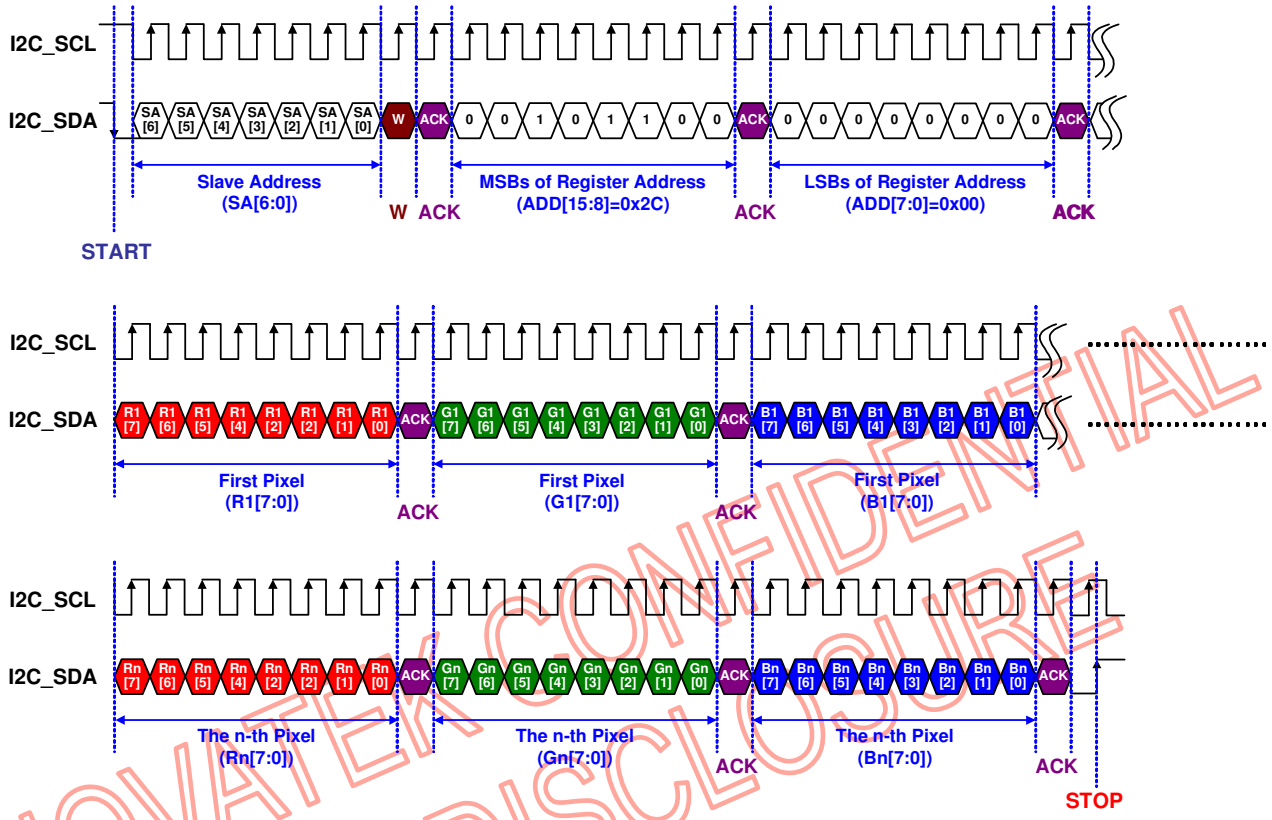
- 262K colors, RGB is 6-6-6-bit pixel data input (parameter of command 3A00h is 0x0006)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[5:0], R2[5:0], ···, Rn[5:0]: The red color data of each pixel
G1[5:0], G2[5:0], ···, Gn[5:0]: The green color data of each pixel
B1[5:0], B2[5:0], ···, Bn[5:0]: The blue color data of each pixel

- 16.7M colors, RGB is 8-8-8-bit pixel data input (parameter of command 3A00h is 0x0007)



W: Write Bit, where W="0"
ACK: Acknowledge Bit, where ACK="0"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2C00"
R1[7:0], R2[7:0], ···, Rn[7:0]: The red color data of each pixel
G1[7:0], G2[7:0], ···, Gn[7:0]: The green color data of each pixel
B1[7:0], B2[7:0], ···, Bn[7:0]: The blue color data of each pixel

5.2.4 Register Read Sequence of I2C Interface

NT35510 supports register read sequence via I2C-bus transfer. Register data reading transfers follow the format and is shown in Fig.5.2.4.

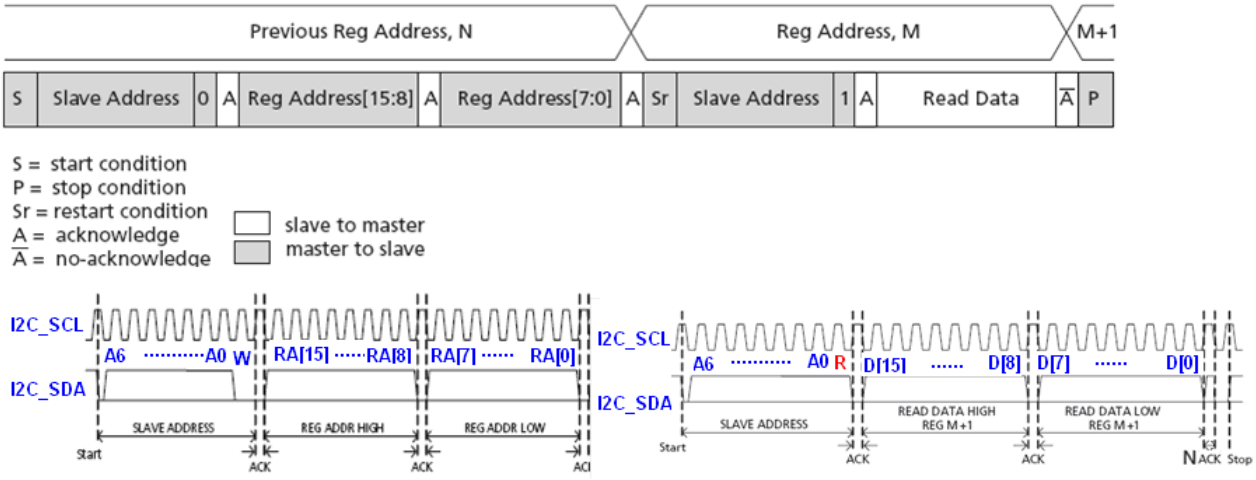


Fig. 5.2.4 Register Reading Timing of I2C Interface

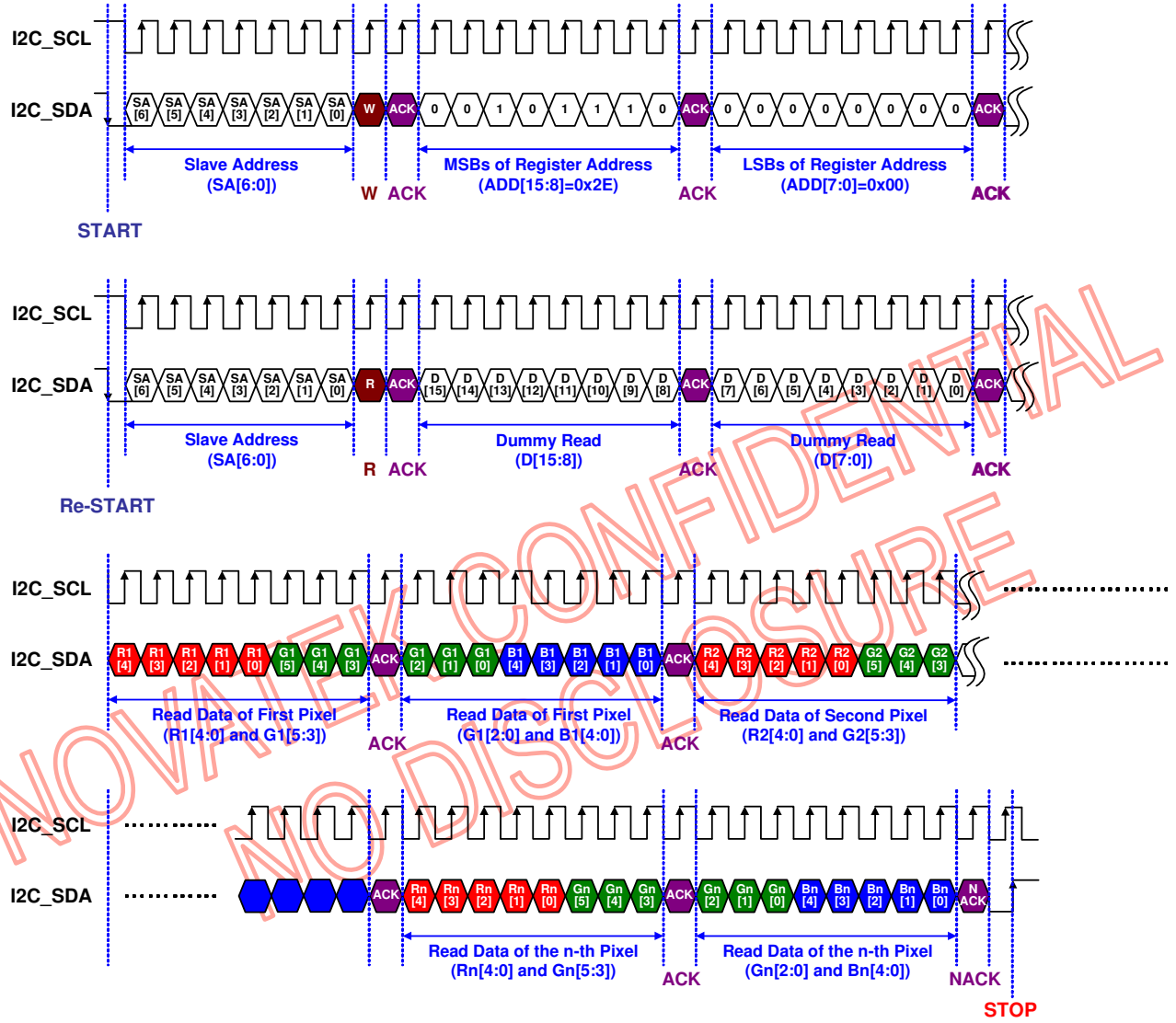
5.2.5 RAM Data Read Sequence of I2C Interface

NT35510 supports RAM data read function for I2C interface.

The master MCU need to send the RAM address of reading first and transfer protocol can refer to the 5.2.3 Register Write Sequence. Then the master MCU need to send the RAM data read register "2E00h" to NT35510. And finally, the MCU can send the following RAM data reading timing to feedback single RAM data value by one complete I2C packet.

The RAM data reading timing is shown in below.

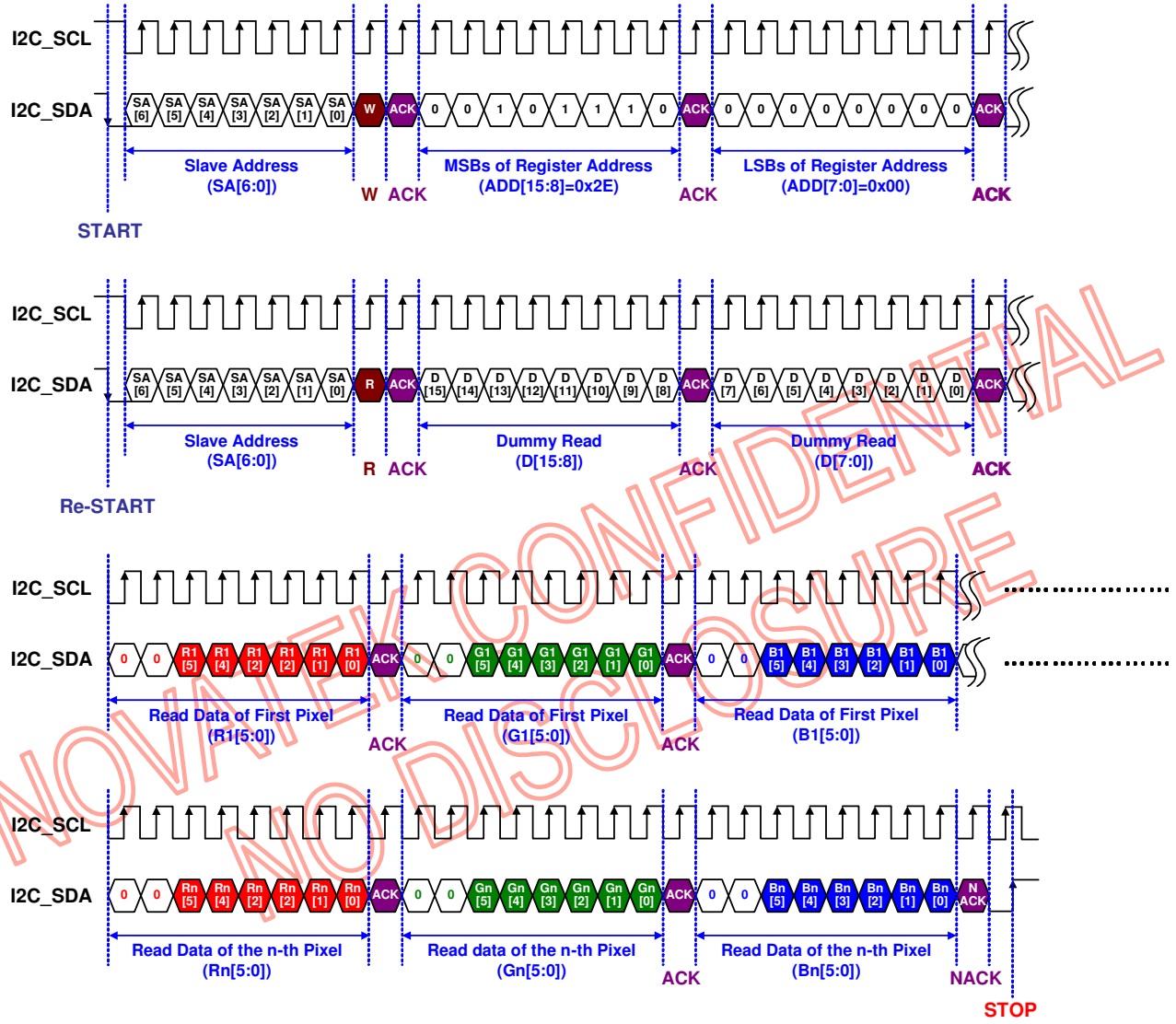
- 65K colors, RGB is 5-6-5-bit pixel data output (parameter of command 3A00h is 0x0005)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[4:0], R2[4:0], ···, Rn[4:0]: The red color data of each pixel
G1[5:0], G2[5:0], ···, Gn[5:0]: The green color data of each pixel
B1[4:0], B2[4:0], ···, Bn[4:0]: The blue color data of each pixel

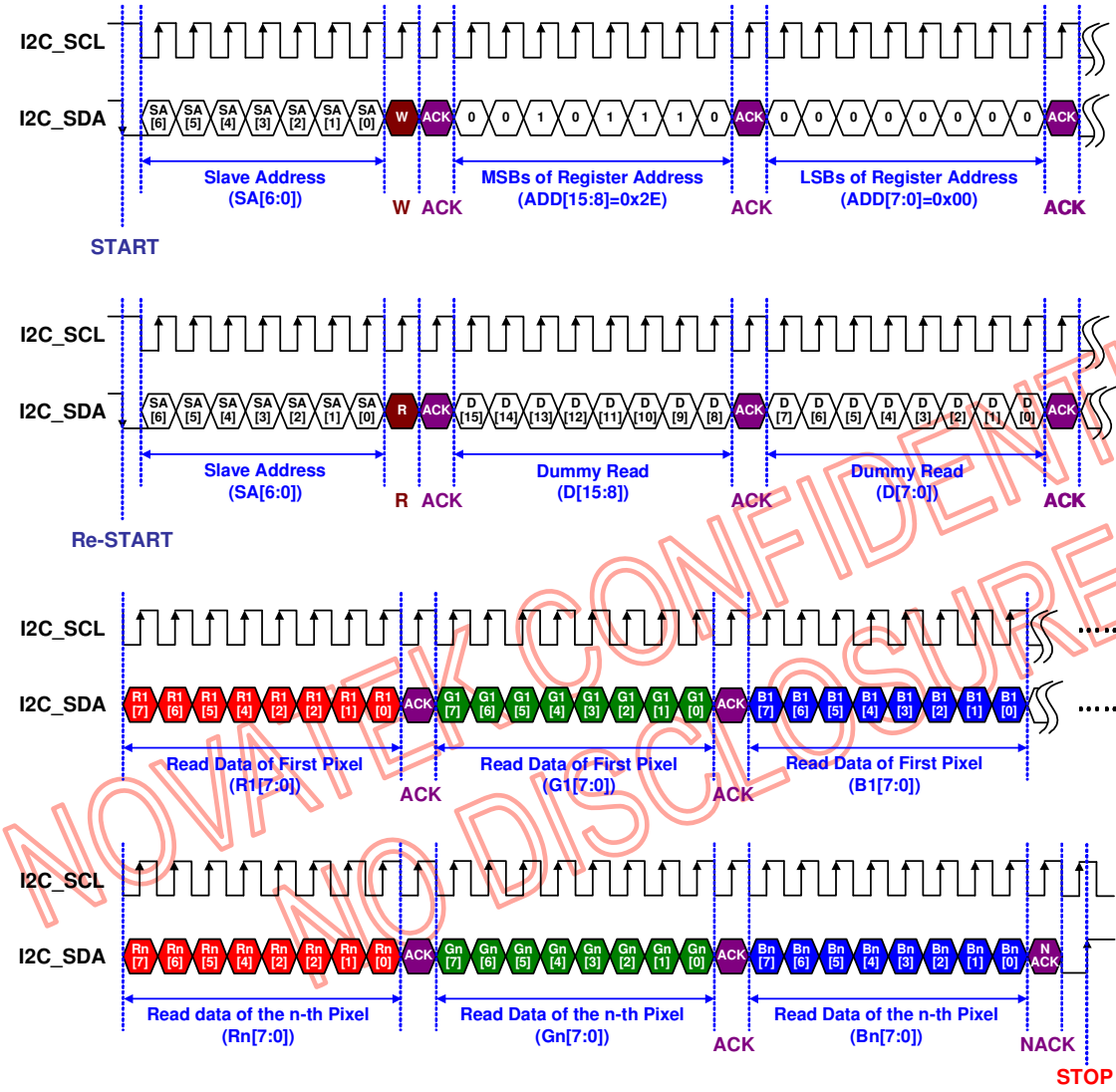
- 262K colors, RGB is 6-6-6-bit pixel data output (parameter of command 3A00h is 0x0006)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[5:0], R2[5:0], ···, Rn[5:0]: The red color data of each pixel
G1[5:0], G2[5:0], ···, Gn[5:0]: The green color data of each pixel
B1[5:0], B2[5:0], ···, Bn[5:0]: The blue color data of each pixel

- 16.7M colors, RGB is 8-8-8-bit pixel data output (parameter of command 3A00h is 0x0007)



W: Write Bit, where W="0"
R: Read Bit, where R="1"
ACK: Acknowledge Bit, where ACK="0"
NACK: Non-acknowledge Bit, where NACK="1"

SA[6:0]: Slave Address
ADD[15:0]: Register Address, where ADD[15:0]="0x2E00"
R1[7:0], R2[7:0], ···, Rn[7:0]: The red color data of each pixel
G1[7:0], G2[7:0], ···, Gn[7:0]: The green color data of each pixel
B1[7:0], B2[7:0], ···, Bn[7:0]: The blue color data of each pixel

5.3 Interface Pause

By using parallel interface, it is possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the CSX (Chip Select Line) is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then NT35510 will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the CSX (Chip Select Line) is released after a whole byte of a command as been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the CSX (Chip Select Line) is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Parallel Interface Pause

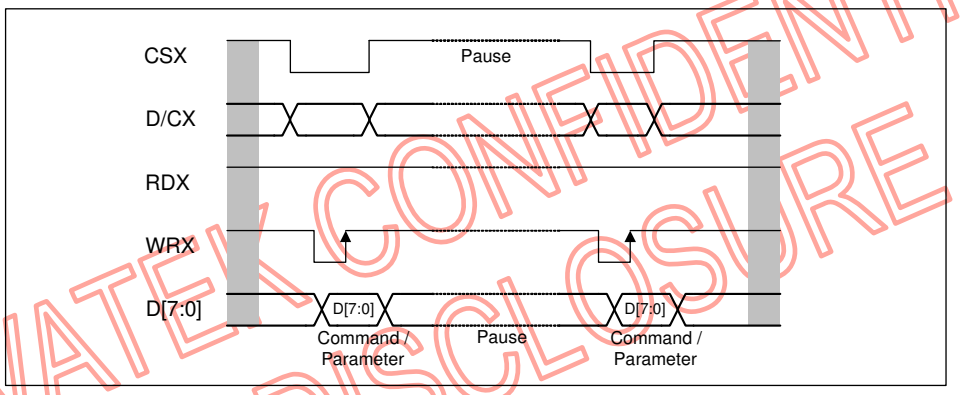


Fig. 5.3.1 Parallel bus protocol, write mode – paused by CSX

Serial Interface Pause

16-bit SPI interface does not support "Pause Mode"

MIPI Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.
1) Same receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => …
2) Different receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => …

The means that "=>" symbol means a pause on DSI.

5.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example (See ***Fig. 5.4.1***)

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then NT35510 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example (See ***Fig. 5.4.2***)

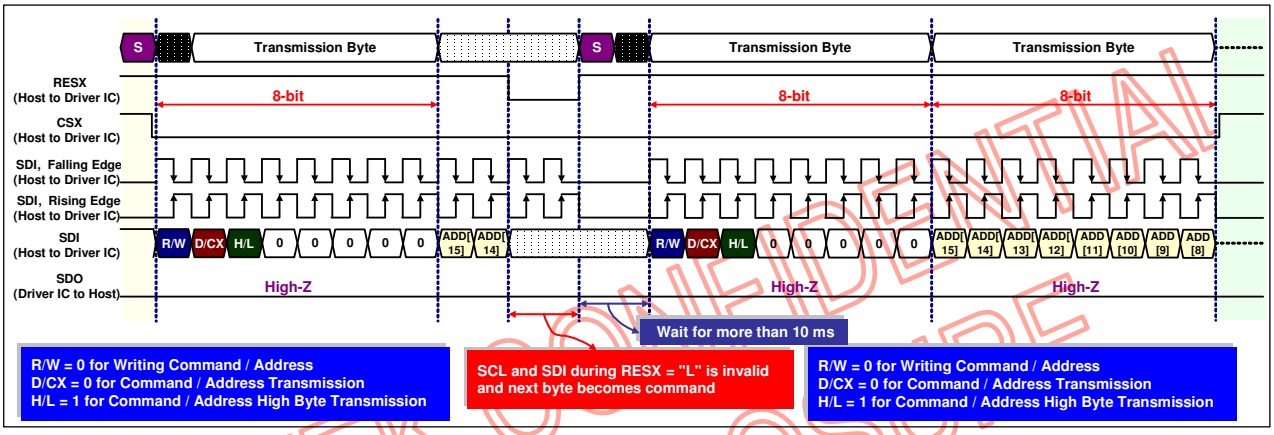


Fig. 5.4.1 Serial bus protocol, write mode – interrupted by REX

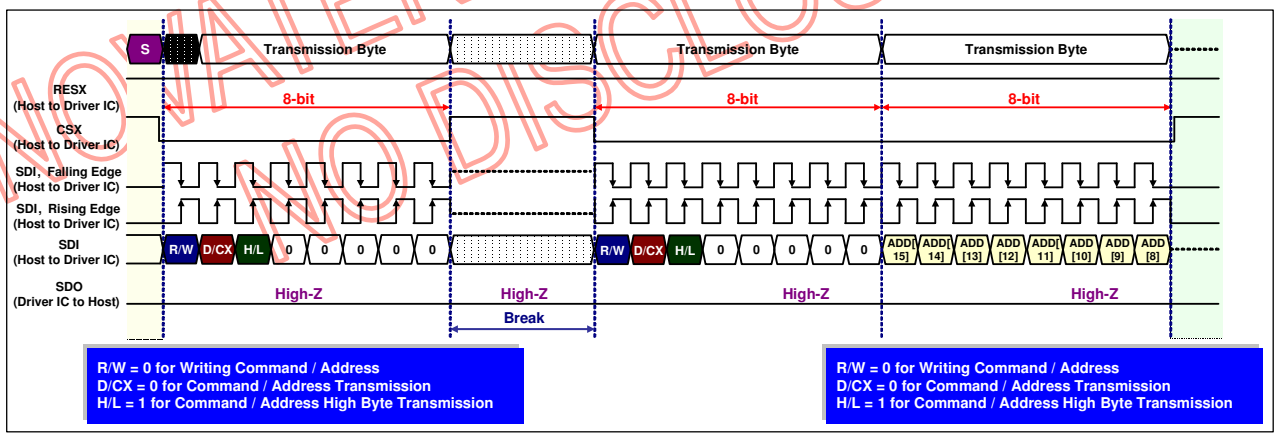
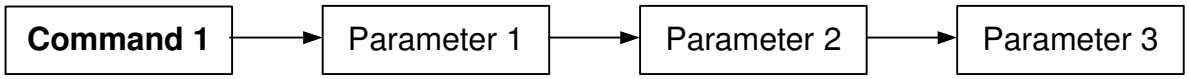


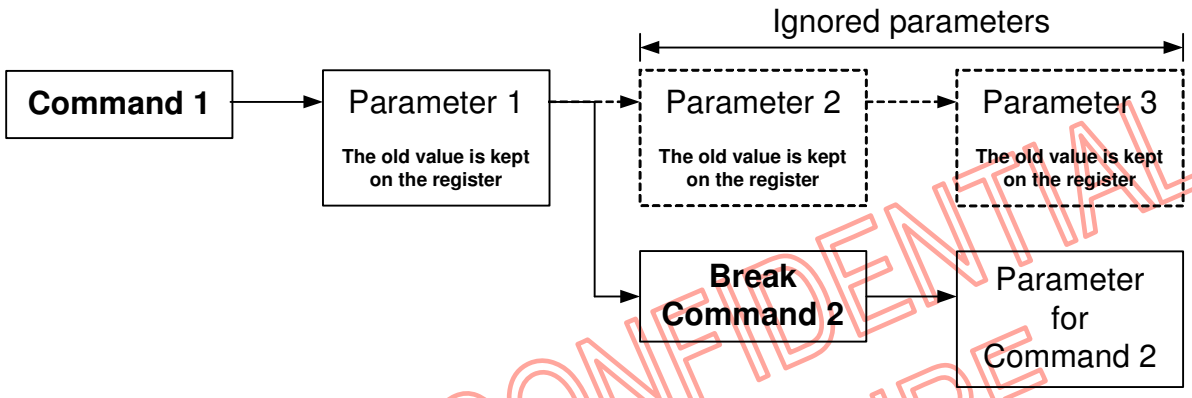
Fig. 5.4.2 Serial bus protocol, write mode – interrupted by CSX

Display data transfer break is illustrated for reference purposes below.

Without break



With break (See and check also exceptions*)



Break can be e.g. another command or noise pulse.

Fig. 5.4.3 Break during Parameter

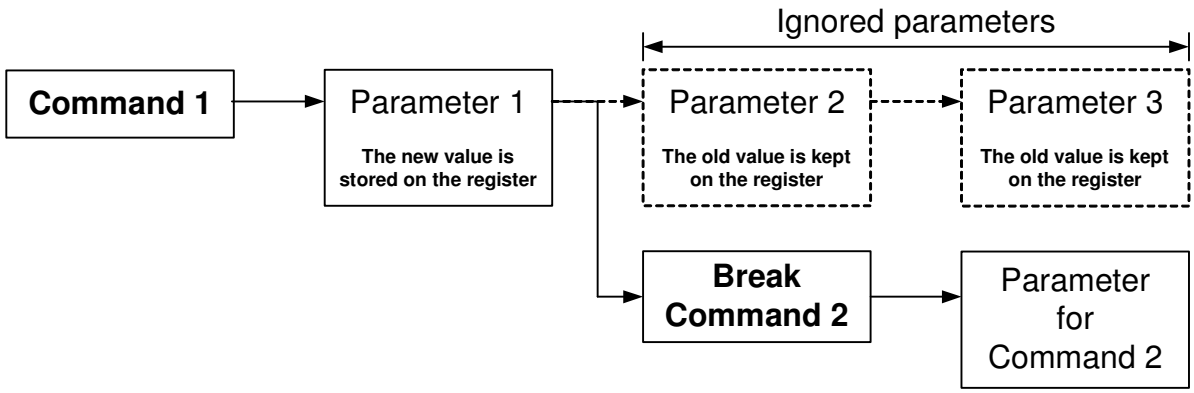
*) See also an exception on section "6.1 User Command Set" and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

The NT35510 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

Except MIPI interface, the data transfer break mechanism illustrated for reference purposes below.



5.5 Display Module Data Transfer Modes

The NT35510 has 3 kinds of color mode for transferring data to the frame Memory. There are 16-bit color per pixel, 18-bit color per pixel and 24-bit color per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

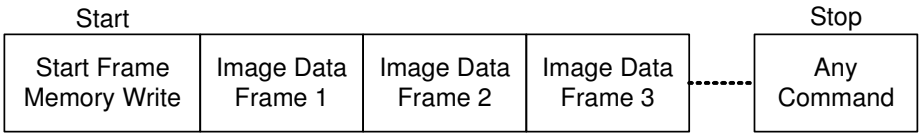


Fig. 5.5.1 Data Transfer Method 1

Method 2

Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.

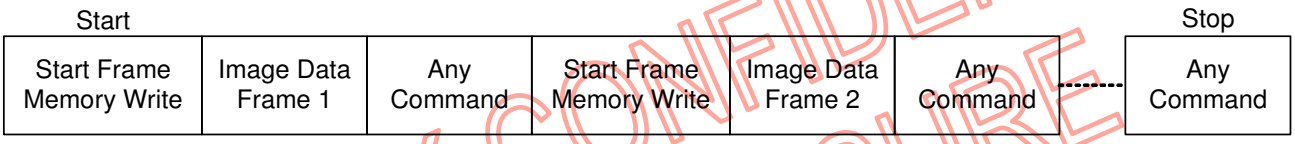


Fig. 5.5.2 Data Transfer Method 2 with "Start Frame Memory Write" Break

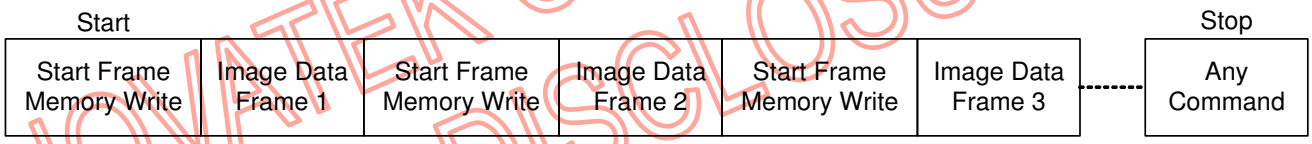


Fig. 5.5.3 Data Transfer Method 2 with "Any Command" Break

NOTES:

1) The Frame Memory can contain odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

2) "Memory Write Continue (3Ch)" or "Memory Read Continue (3Eh)" commands are not stopping writing or reading to/from the frame memory. These commands can be used if there is wanted to continue the writing or reading to/from the frame memory when "Any Command" has stopped the memory writing or reading.

3) "Any Command" can be as same as "Start Frame Memory Write".

5.6 RGB Interface

5.6.1 General Description

For direct interface with both graphic controller and MPU, NT35510 offer RGB interface mode to display video signal. The parallel RGB interface includes: VS, HS, DE, PCLK, D[23:0]. The interface is activated after Power On sequence (See section Power On/Off Sequence)

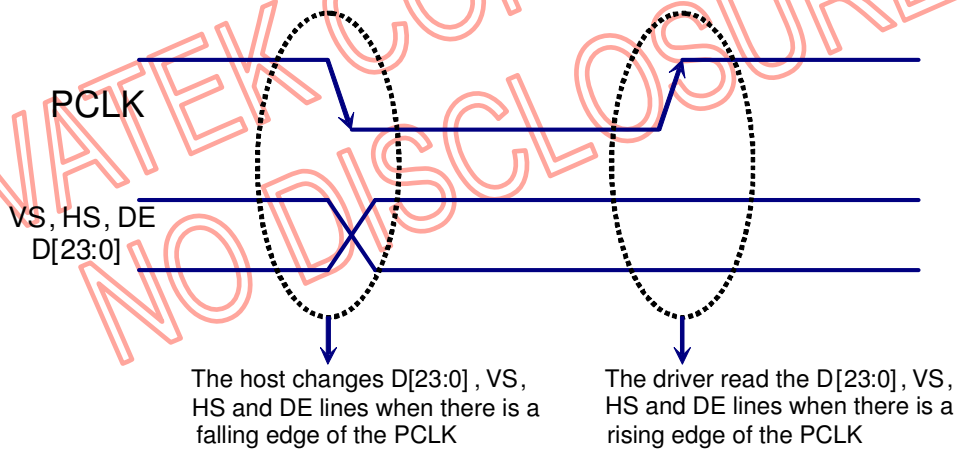
Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, DE and D[23:0] states when there is a rising edge of the PCLK. The PCLK cannot be used as continues internal clock for other functions of the display module e.g. Sleep In –mode etc.

Vertical synchronization (VS) is used to tell when there is received a new frame of the display. This is negative (“0”, low) active and its state is read to the display module by a rising edge of he PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is negative (“0”, low) active and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a positive (“1”, high) active and its state is read to the display module by a rising edge of the PCLK signal. D[23:0] (24-bit: R7-R0, G7-G0 and B7-B0;18-bit: R5-R0, G5-G0 and B5-B0; 16-bit: R4-R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (When DE= “1” and there is a rising edge of PCLK). D[23:0] can be “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK signal.

The PCLK cycle is described in the follow figure.



Note: PCLK is an unsynchronized signal (It can be stopped)

5.6.2 RGB Interface Timing Chart

The image information must be correct on the display, when the timings are in range on the interface.
However, the image information can be incorrect on the display, when timings are not out of range on the interface (Out of the range timings cannot on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.) when there is returned from out of the range to in range interface timing.

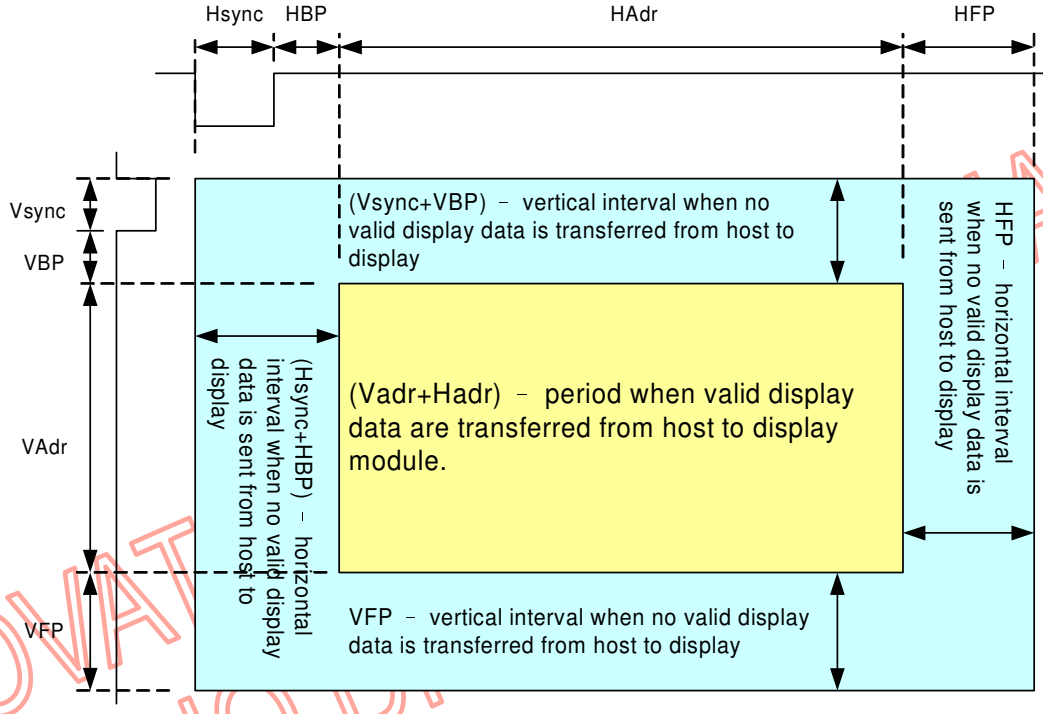


Fig. 5.6.1 RGB interface general timing diagram

5.6.3 RGB Interface Mode Set

RGB I/F Mode	PCLK	DE	D23-D0	VS	HS	Register VFP[7:0], VBP[7:0] HFP[7:0], HBP[7:0]
RGB Mode 1 (SYNC + DE)	Used	Used	Used	Used	Used	Not used
RGB Mode 2 (SYNC only)	Used	Not used	Used	Used	Used	Used

In RGB Mode 1, writing data to line buffer is done by PCLK and Video Data Bus (D23 to D0), when DE is high state. The external clocks (PCLK, VS and HS) are used for internal displaying clock. So, controller must always transfer PCLK, VS and HS signal to NT35510 DDI.

In RGB Mode 2, back porch of Vsync VBP is defined by VBP[7:0] of RGBCTR command. And back porch of Hsync HBP is defined by HBP[7:0] of RGRCTR command. Front porch of Vsync VFP is defined by VFP[7:0] of RGBCTR command. And front porch of Hsync HFP is defined by HFP[7:0] of RGBCTR command.

Note: VBP[7:0]=Vsync+VBP and HBP[7:0]=Hsync+HBP.

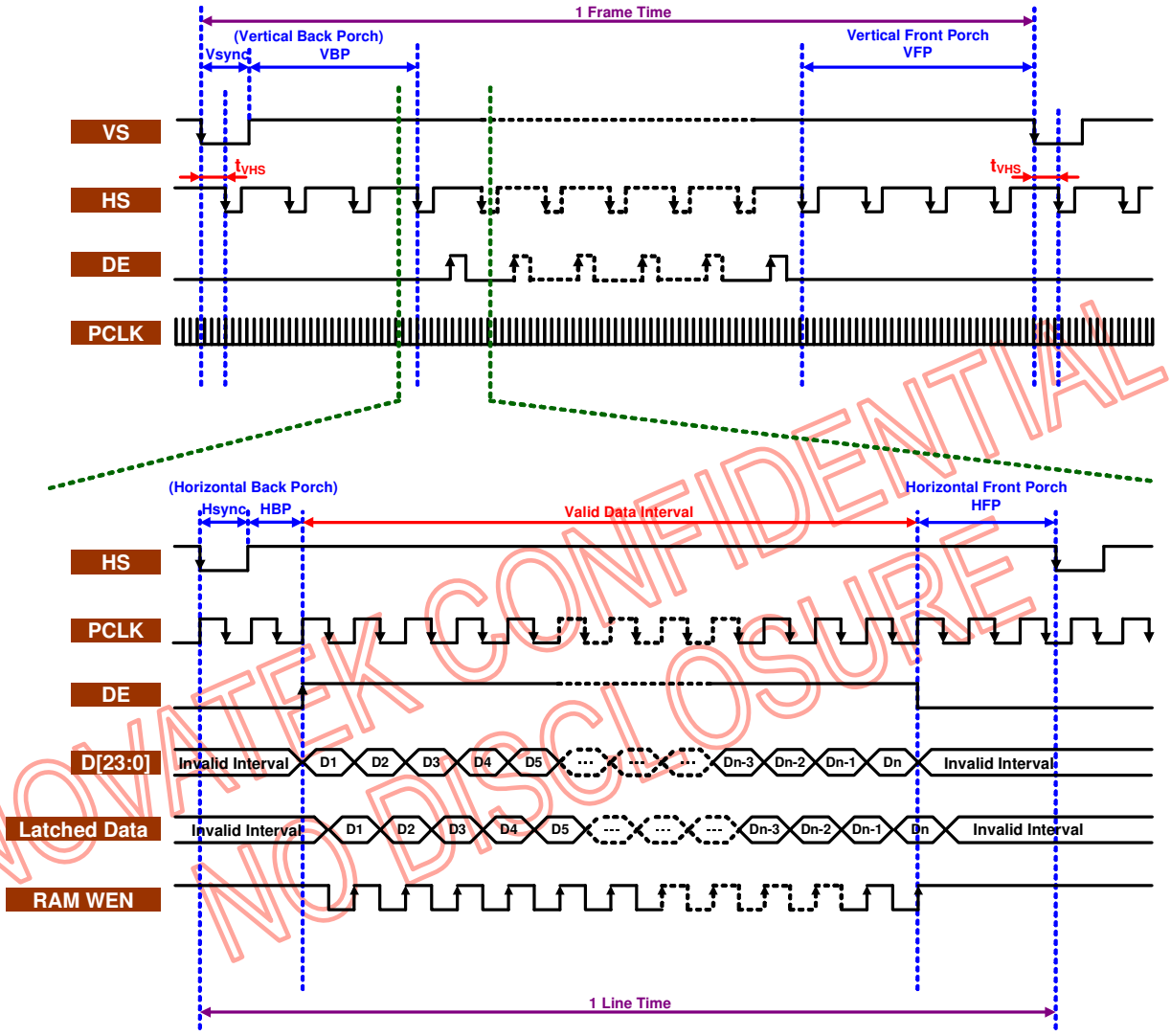


Fig. 5.6.2 Video signal data writing method in RGB Mode 1 Interface

Notes:

1. Constraint:

V-Back Porch (Vsync+VBP)≧ 5 HS lines, V-Front-Borch (VFP) ≧ 2 HS lines

Vsync+VBP+VFP (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch)

H-Back Porch (Hsync+HBP)≧ 5 PCLK clocks, H-Front-Porch (HFP) ≧ 2 PCLK clocks

2. t_{VHS}≧400ns

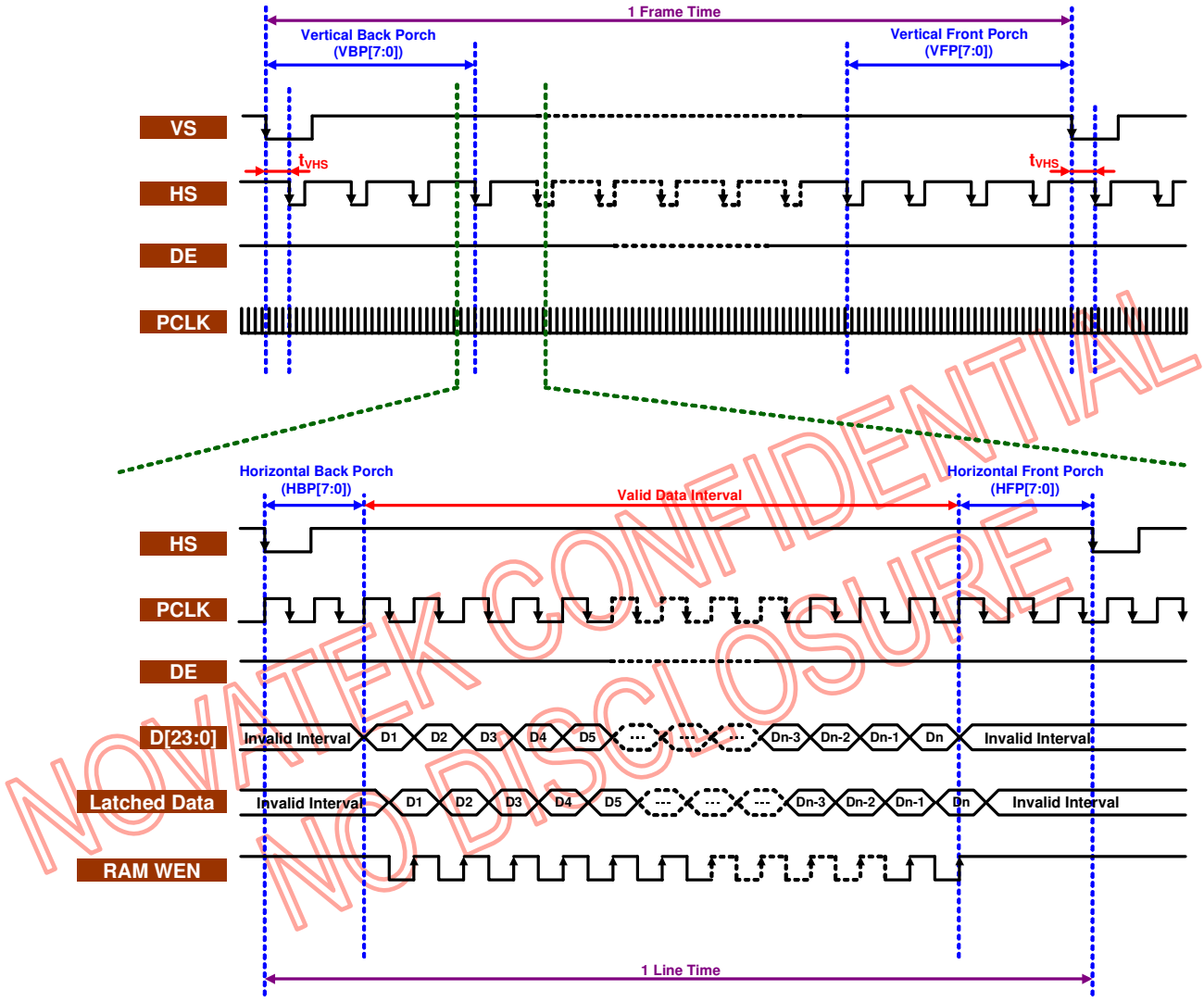


Fig. 5.6.3 Video signal data writing method in RGB Mode 2 Interface

Notes:

1. Constraint:

V-Back Porch (VBP[7:0]) ≧ 5 HS lines, V-Front Porch (VFP[7:0]) ≧ 2 HS lines

VBP[7:0]+VFP[7:0] (porch of RGB signal) > VBPA/B/C[7:0] (internal display back porch)

H-Back Porch (HBP[7:0]) ≧ 5 PCLK clocks, H-Back Porch (HFP[7:0]) ≧ 2 PCLK clocks

2. t_{VHS}≧400ns

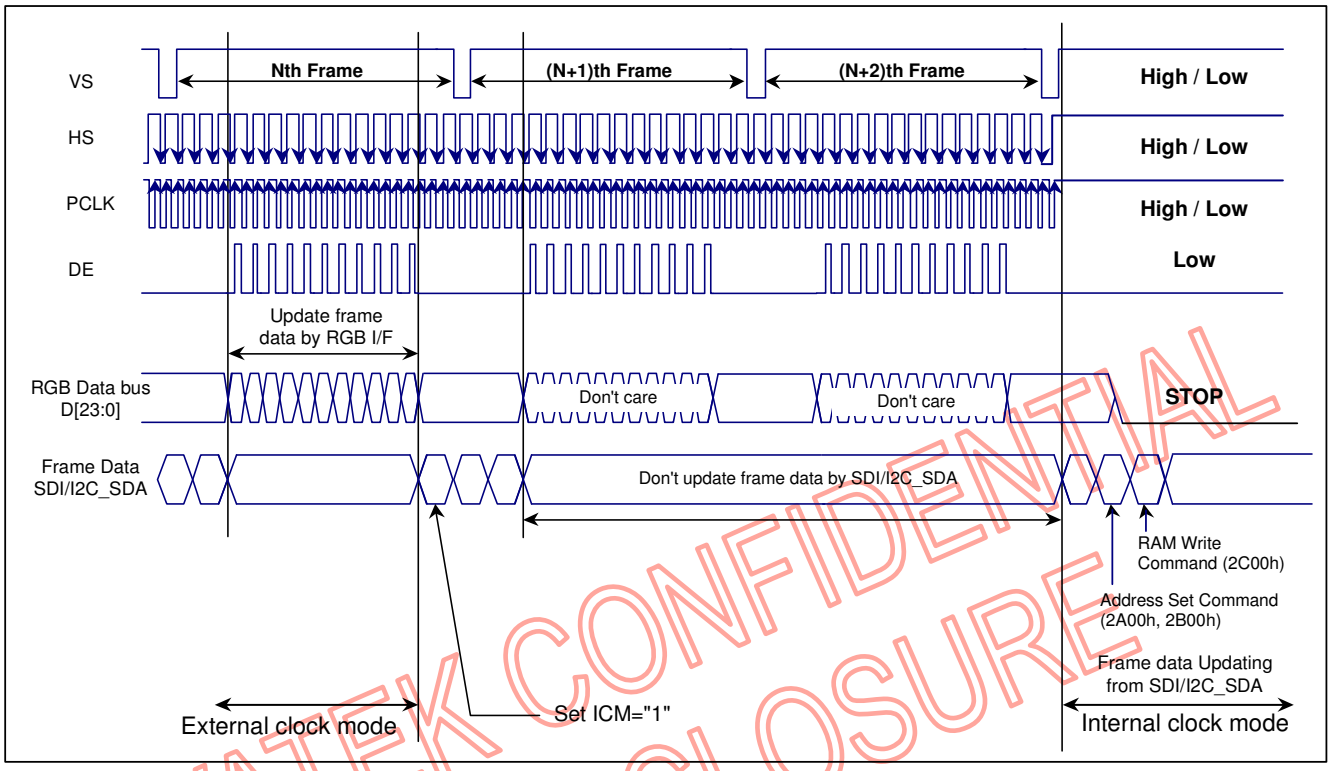


Fig. 5.6.4 RGB with SPI Timing Sequence (Enter Internal Clock Mode, ICM="1")

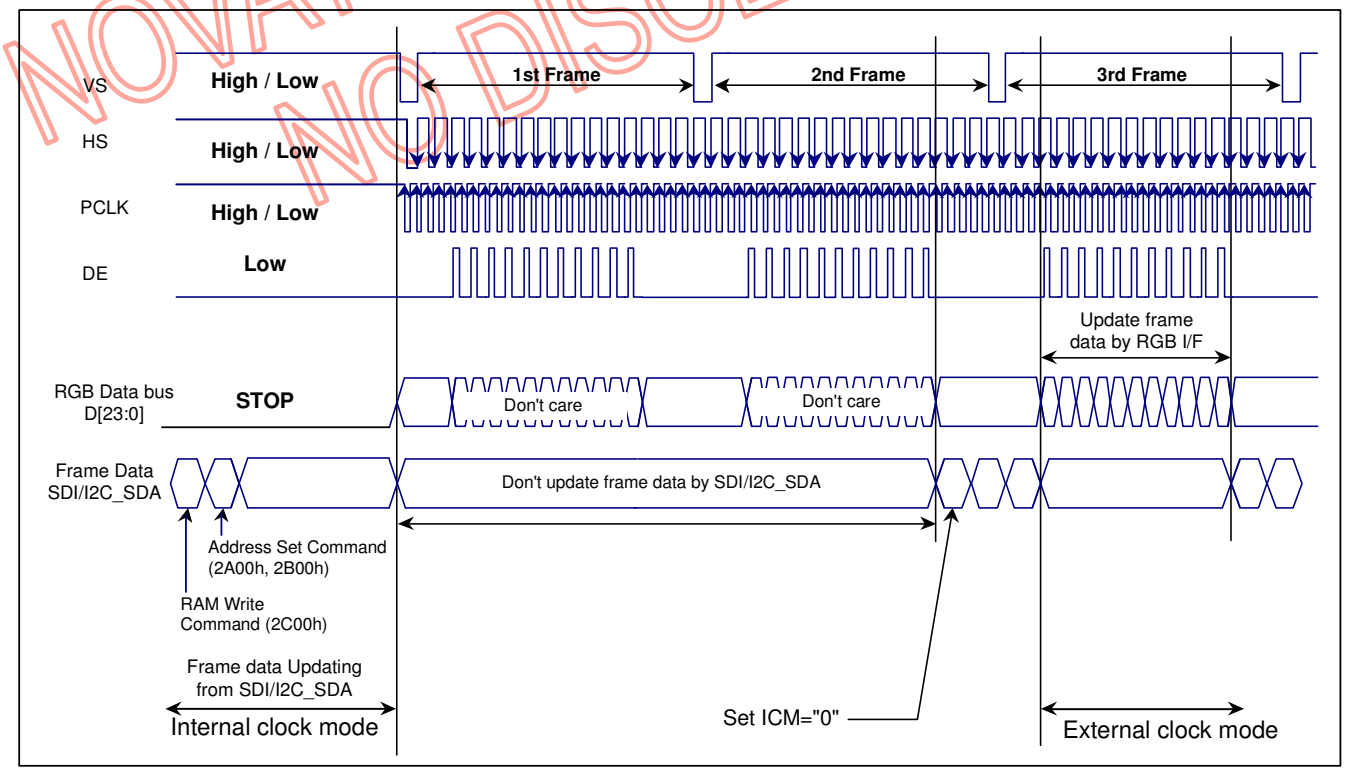


Fig. 5.6.5 RGB with SPI Timing Sequence (Exit Internal Clock Mode, ICM="0")

5.6.4 RGB Interface Bus Width Set

All 3-kinds of bus width can be available during RGB interface mode (selected by the COLMOD command (3A00h): VIPF[3:0]).

3A00h	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Bus Width
50h	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	16-bit data
60h	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	18-bit data
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit data

NOTES:

1. "x": Unused RGB data bus connected with VSSI.

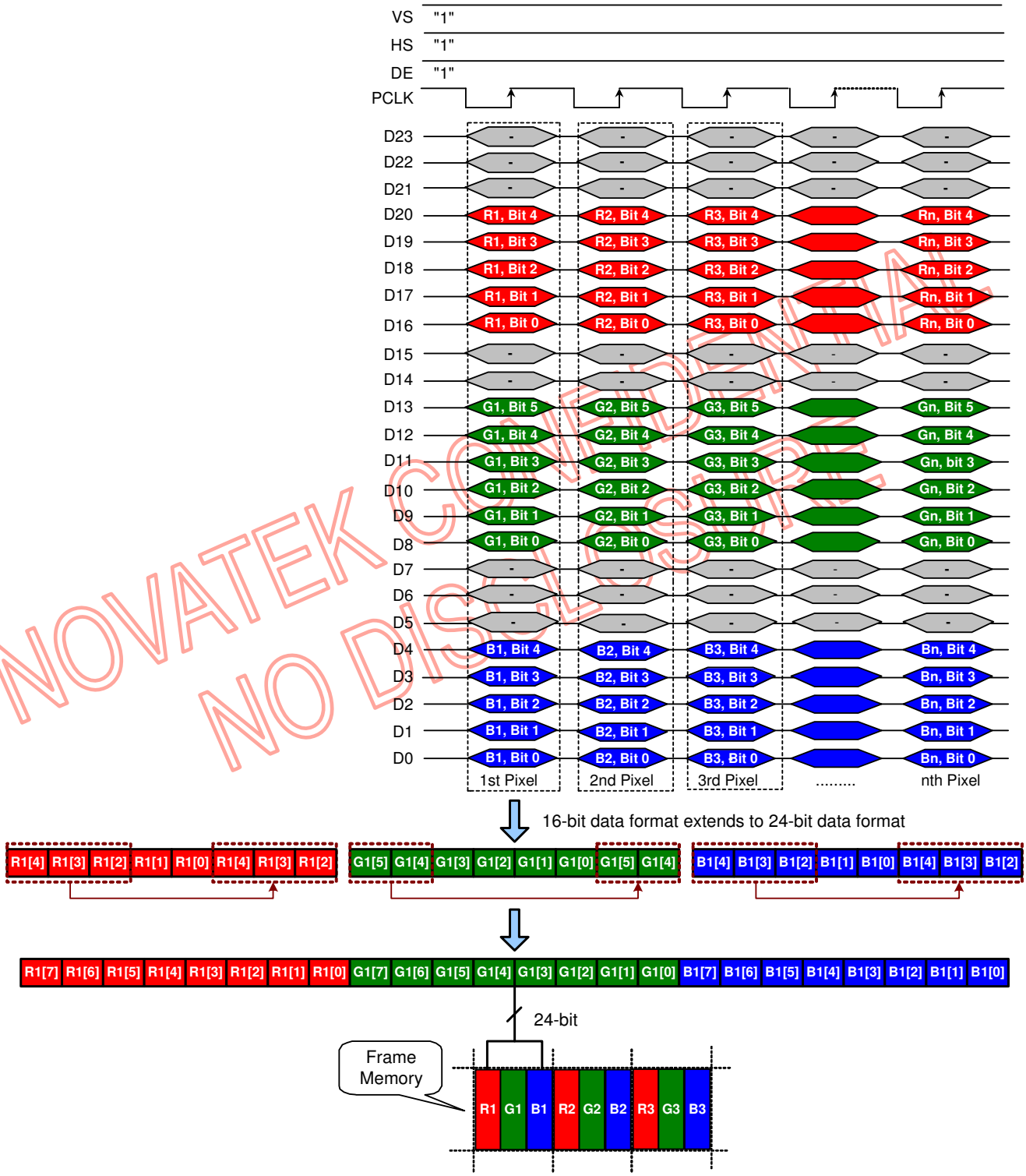
2. R0 is the LSB for the red component; G0 is the LSB for the green component, etc.

3. For 16-bit pixels, R primary color MSB is R4, G primary color MSB is G5 and B primary color MSB is B4.

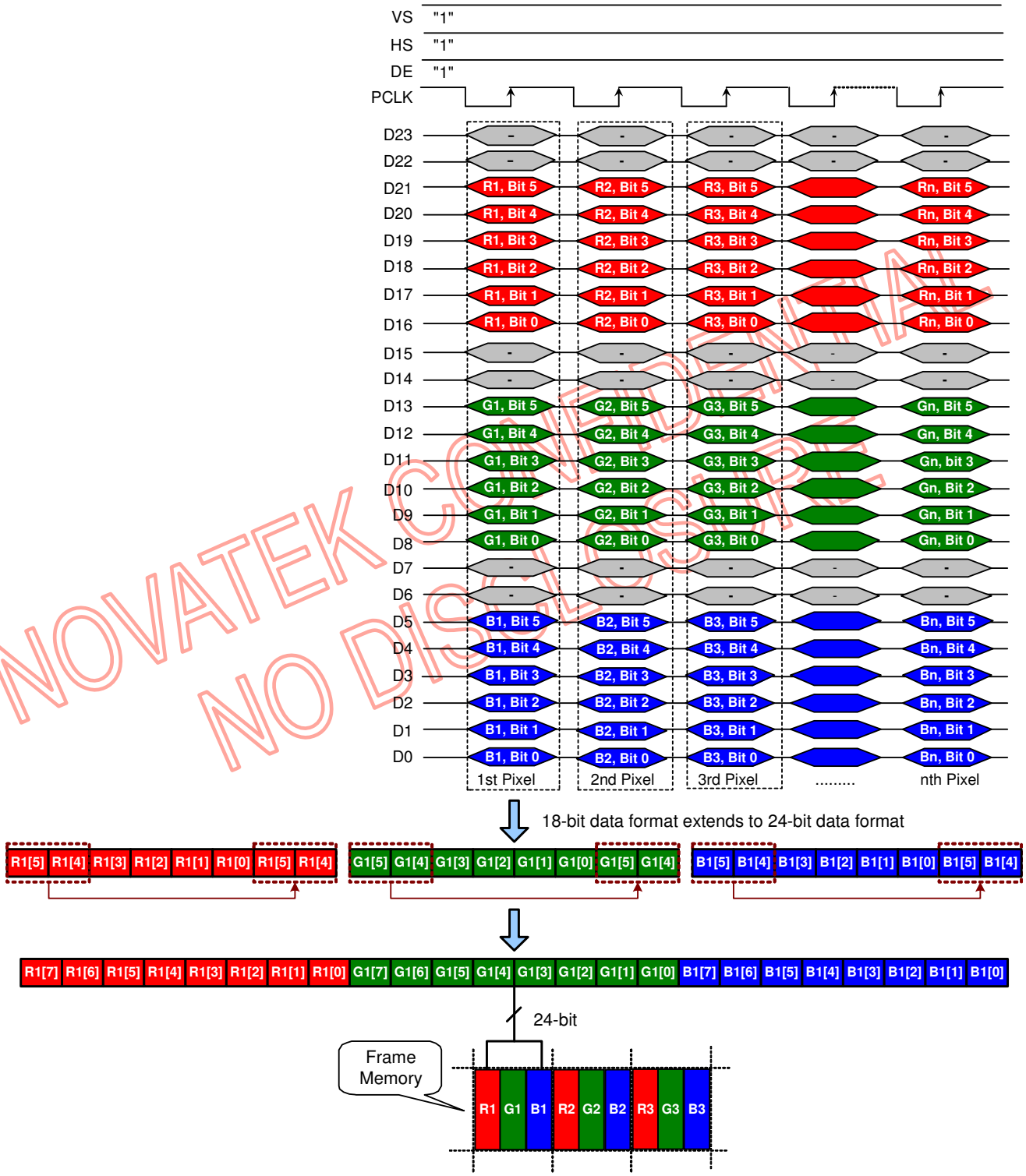
4. For 18-bit pixels, R primary color MSB is R5, G primary color MSB is G5 and B primary color MSB is B5.

5. For 24-bit pixels, R primary color MSB is R7, G primary color MSB is G7 and B primary color MSB is B7

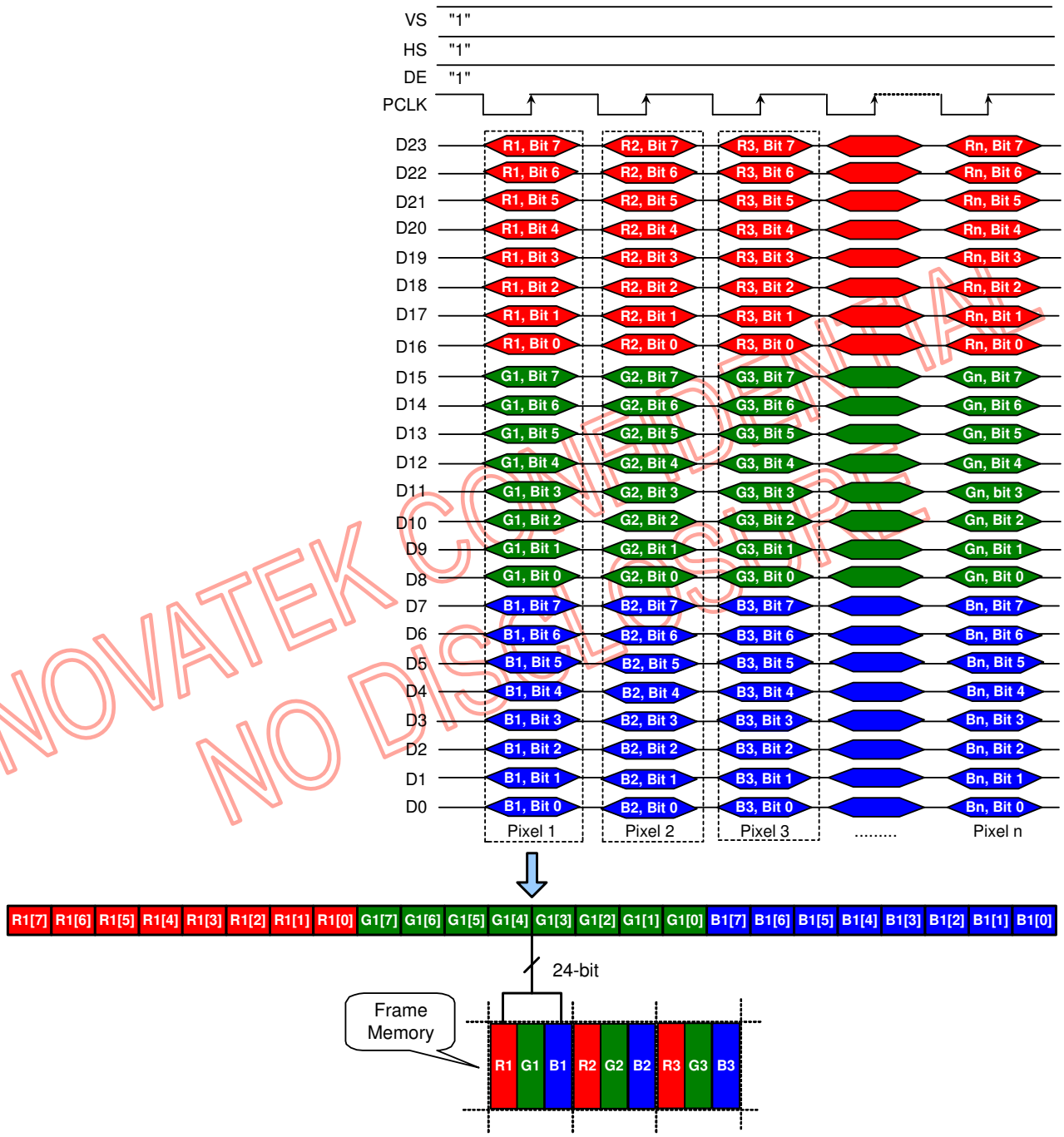
Write data for 16-bit RGB interface bus width set is shown below.



Write data for 18-bit RGB interface bus width set is shown below.



Write data for 24-bit RGB interface bus width set is shown below.

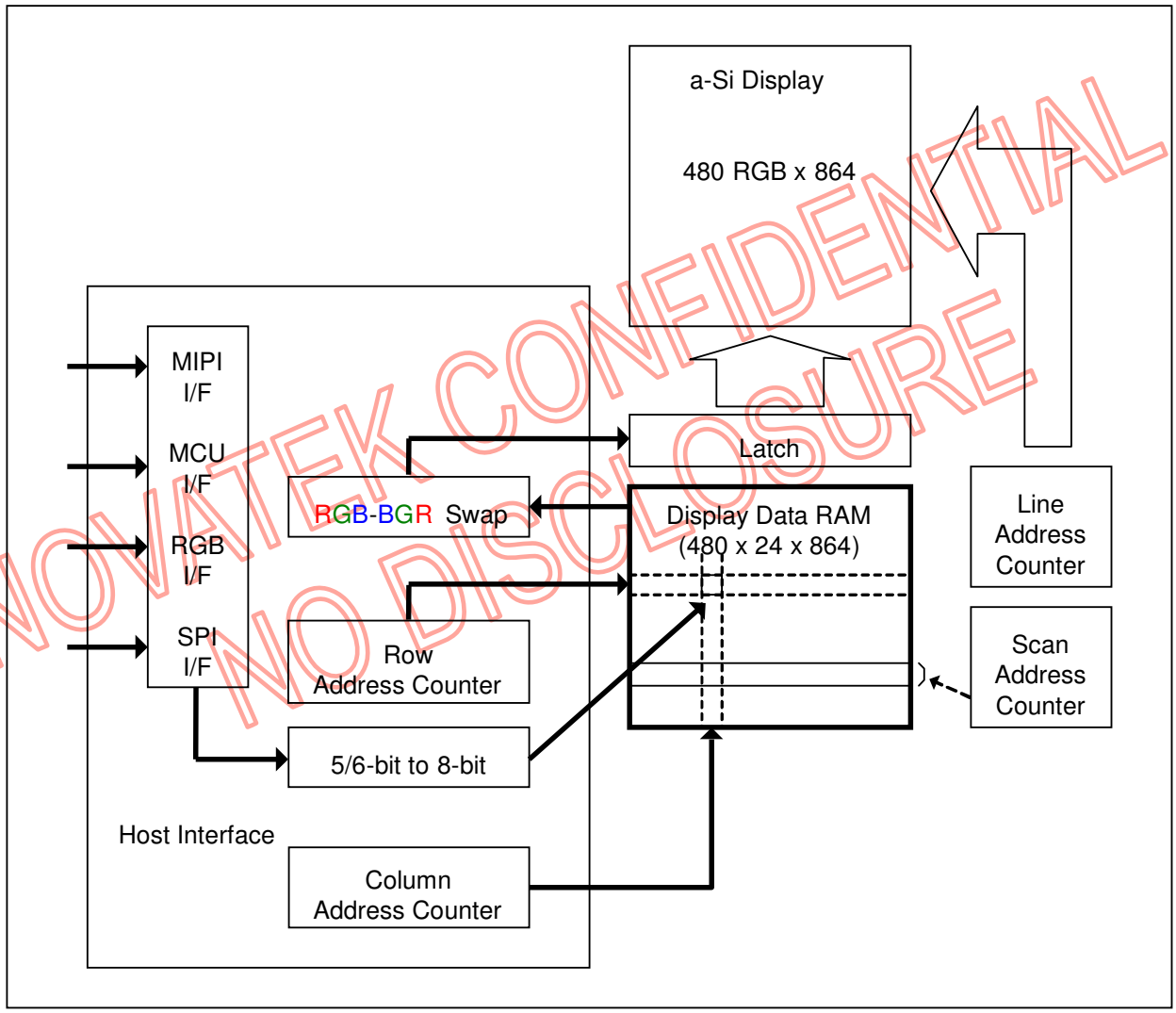


5.7 Frame Memory

5.7.1 Configuration

The NT35510 has an integrated 480 x 864 x 24-bit graphic type static RAM. This 9,953,280-bit memory allows to store on-chip a 480 x RGB x 864, 480 x RGB x 854, 480 x RGB x 800, 480 x RGB x 720 and 480 x RGB x 640 image with an 24-bit resolution (16.7M-color).

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



5.7.2 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 1-1-1-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The address pointers address the locations of RAM.

When CGM[7:0]=”70h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=863 (35Fh).
When CGM[7:0]=”6Bh”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=853 (355h).
When CGM[7:0]=”50h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=799 (31Fh).
When CGM[7:0]=”28h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=719 (2CFh).
When CGM[7:0]=”00h”, the address ranges are X=0 to X=479 (1DFh) and Y=0 to Y=639 (27Fh).

Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written when CGM[7:0]=”50h”, if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479 (1DFh), YE=799 (31Fh).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR” (see section 6 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Fig. 5.2.2 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

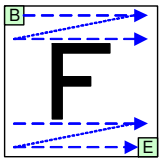
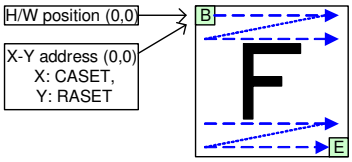
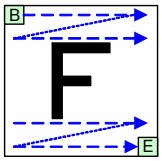
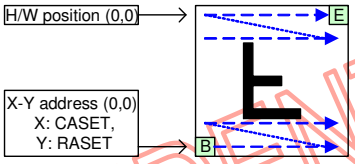
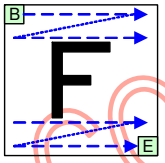
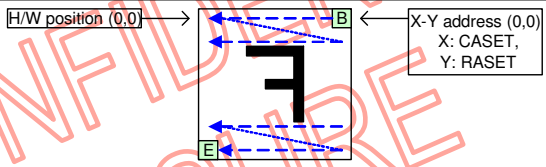
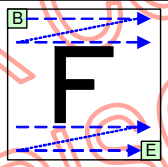
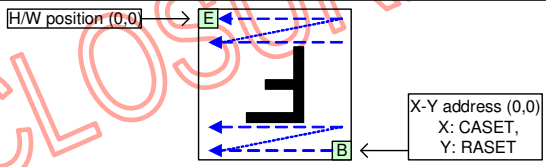
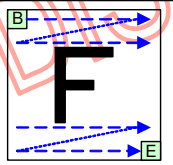
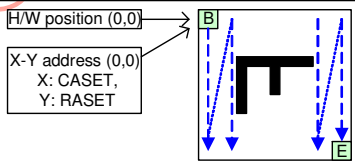
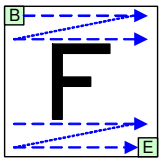
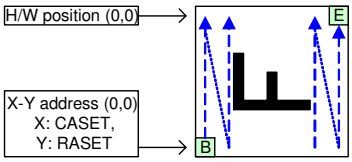
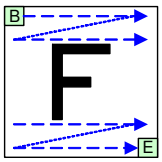
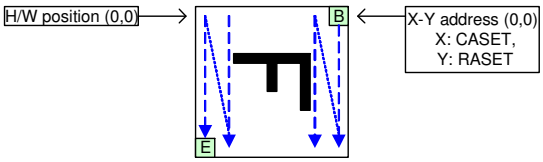
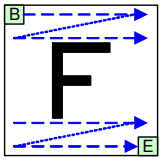
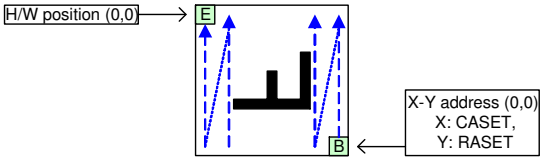
For each image condition, the controls for the column and row counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
Complete Pixel Pair Read / Write action	Twice Increment by 1 (First Pixel n then Pixel n+1)	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

NOTE:
Data is always written to the Frame Memory in the order, regardless of the Memory Write Direction set by command MADCTL (36h) bit MY, MX and MV. The write order for each pixel unit is (R, G, B) transferred from (D2, D1, D0) = (R, G, B). One pixel unit represents 1 column and 1 page counter value on the Frame Memory

5.7.3 Interface to Memory Write Direction

The resultant image for each orientation setting is illustrated below.

Display Data Direction	MADCTR Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

NOTE: MV=D5 parameter of MADCTL command, MX=D6 parameter of MADCTL command, MY=D7 parameter of MADCTL command

5.7.4 Frame Memory to Display Address Mapping

The frame memory to display address mapping for 480RGB x 864 resolution (RSMX=RSMY="0") is shown below figure. The maximum address of RA/SA/CA and used source outputs are decided by bit CGM[2:0] (see command 2Ah CASET, 2Bh PASET and section 7.2).

	Pixel 1			Pixel 2					---	S1433	S1434	S1435	S1436	S1437	S1438	S1439	S1440	
Source Output	S1	S2	S3	S4	S5	S6	S7	S8	----------	S1433	S1434	S1435	S1436	S1437	S1438	S1439	S1440	S1~S1440
	R0	G0	B0	R1	G1	B1	R2	G2	----------	G477	B477	R478	G478	B478	R479	G479	B479	
RA (CA*)	RGB=0 : ⟶ RGB=1 : ⇢																	SA
MY=0	MY=1																	ML=0	ML=1
0	863								----------									0	863
1	862								----------									1	862
2	861								----------									2	861
3	860								----------									3	860
4	859								----------									4	859
5	858								----------									5	858
6	857								----------									6	857
7	856								----------									7	856
8	855								----------									8	855
9	854								----------									9	854
10	853								----------									10	853
11	852								----------									11	852
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
856	7								----------									856	7
857	6								----------									857	6
858	5								----------									858	5
859	4								----------									859	4
860	3								----------									860	3
861	2								----------									861	2
862	1								----------									862	1
863	0								----------									863	0
CA (RA*) MX=0		0			1				----------				478			479			
CA (RA*) MX=1		479			478				----------				1			0			

RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command
ML = Scan direction parameter, D4 parameter of MADCTL command
PTD = Source output voltage selection for 1-bit data "0" and "1", parameter of PWCTR5 command
** RA and CA is exchange when MV = "1"*

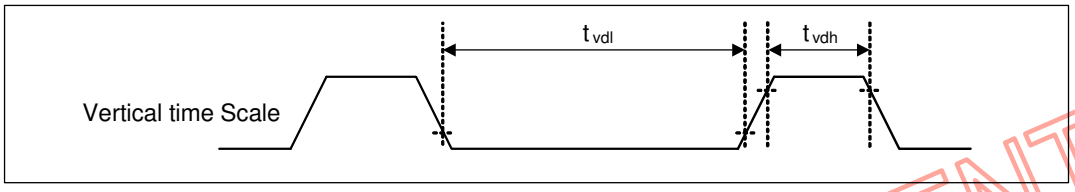
5.8 Tearing Effect Information

5.8.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

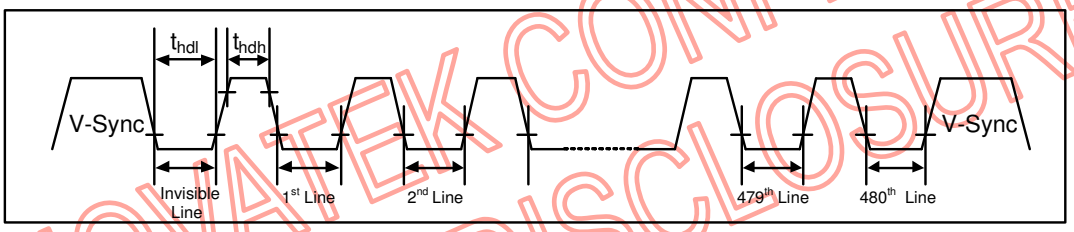
5.8.1.1 TEARING EFFECT LINE MODES

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



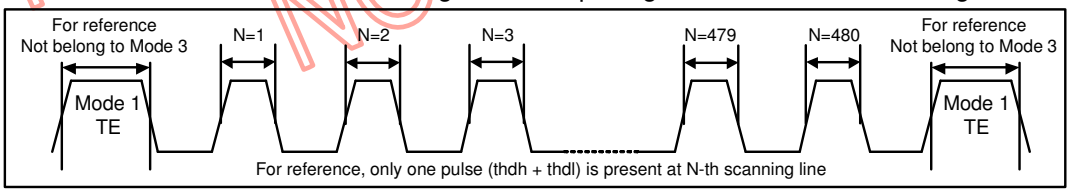
tvdh = The LCD display is not updated from the Frame Memory
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 480 H-sync pulses per field.



thdh = The LCD display is not updated from the Frame Memory
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

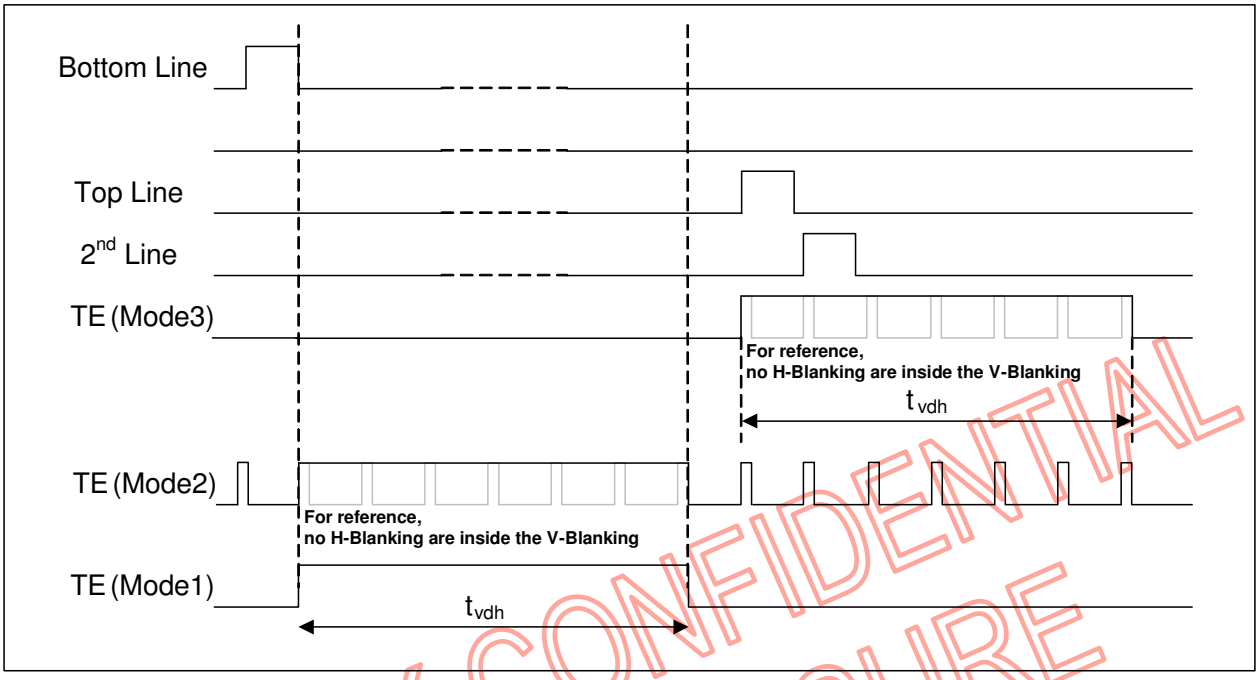
Mode 3, this mode turn on the Tearing Effect Output signal when vertical scanning reaches line N.



N = The N-th scanning line which set by register N[15:0] of command STESL (44h)

The TE mode selection is described as below table

DOPCTR (B100h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	M	N[15:0]	
0	X	X	TE off (output low)
1	34h	X	TE off (output low)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line (Mode 3)
1	35h with M=1	X	TE high in all V-porch and H-porch region (Mode 2)



NOTE: During Sleep In Mode, the Tearing Output Pin is active Low

5.8.1.2 TEARING EFFECT LINE TIMING

The Tearing Effect signal is described below:

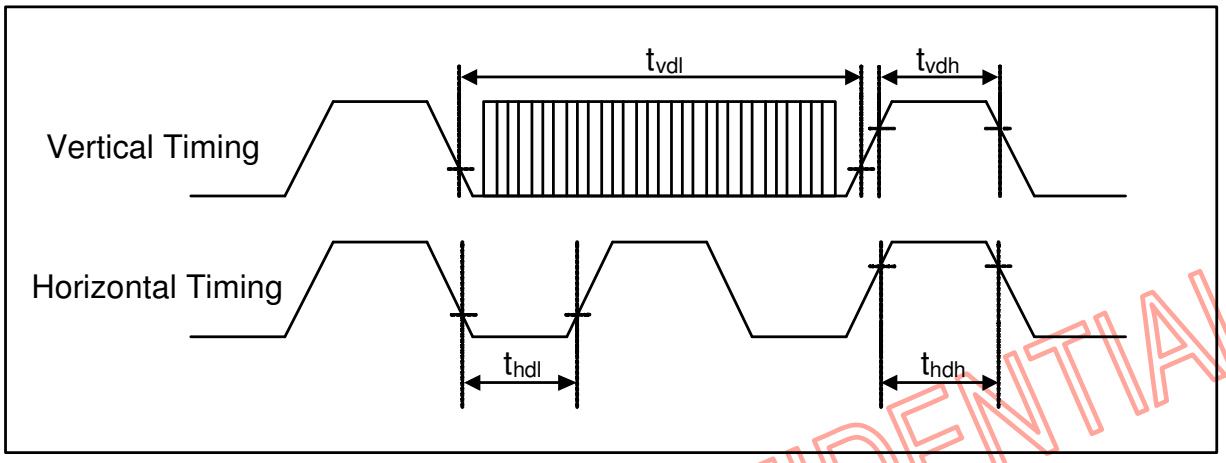


Table 5.8.1 AC characteristics of Tearing Effect Signal

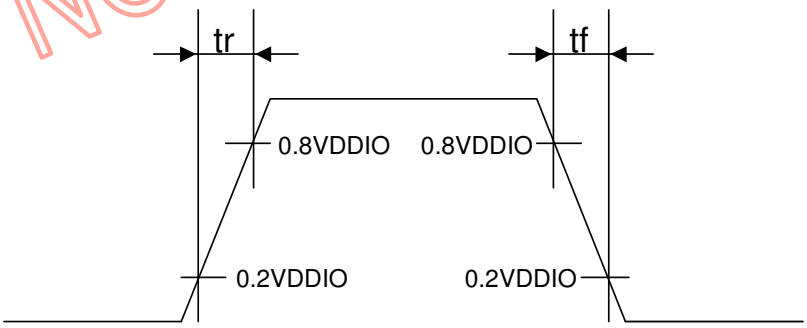
Symbol	Parameter	min	max	unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	TBD	-	µs	
thdh	Horizontal Timing High Duration	TBD	500	µs	

Notes:

1. The timings in above table apply when MADCTL ML=0 and ML=1.

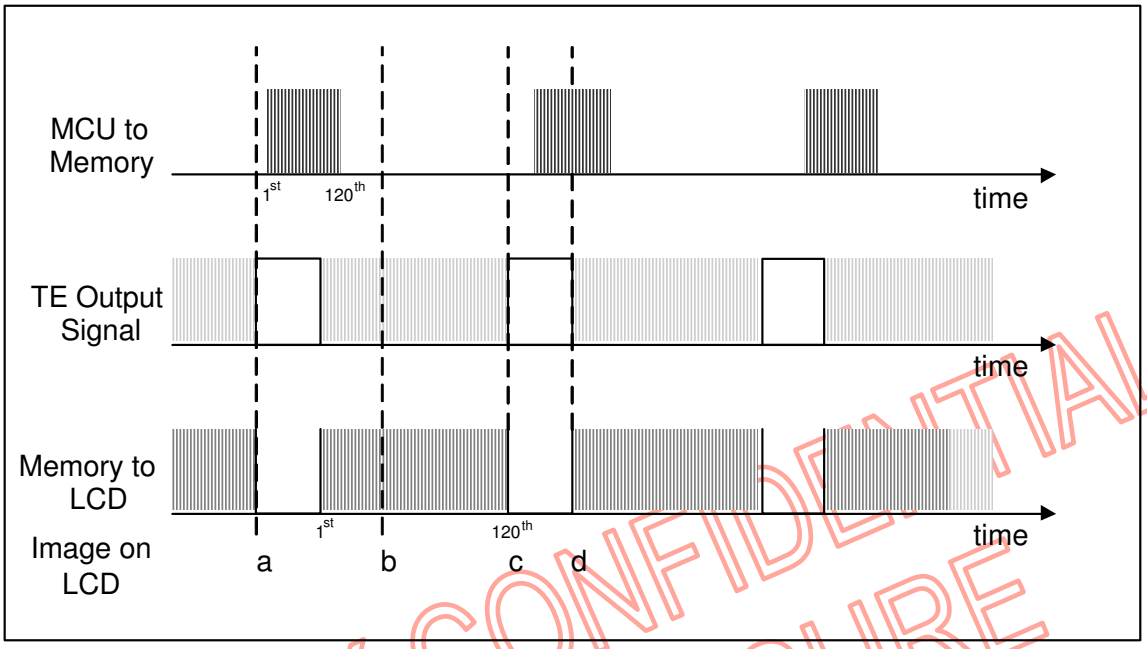
2. The signal's rise and fall times (tr, tf) are stipulated to be equal to or less than 15ns when the maximum load is TBD Ω.

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

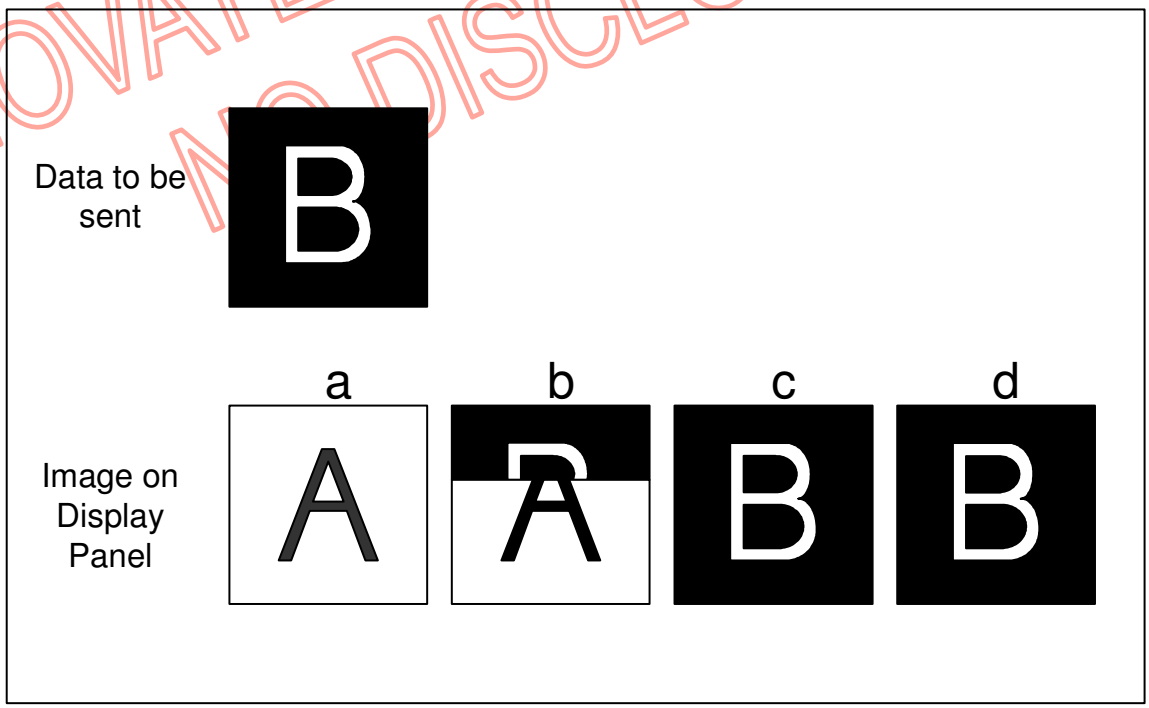


The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

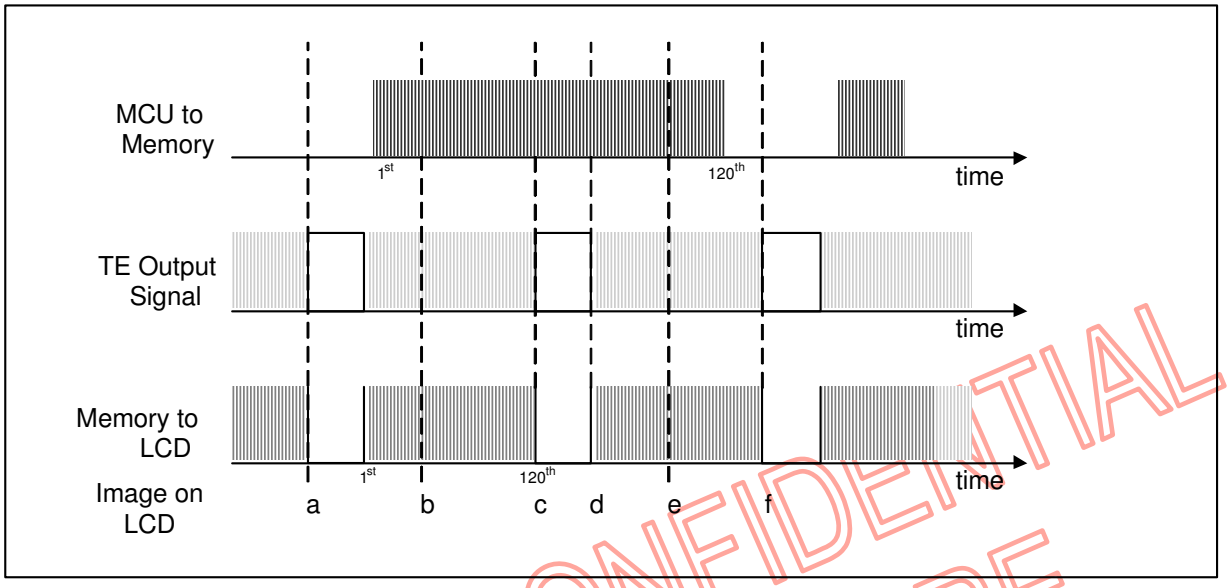
5.8.1.3 EXAMPLE 1: MPU WRITE IS FASTER THAN PANEL READ.



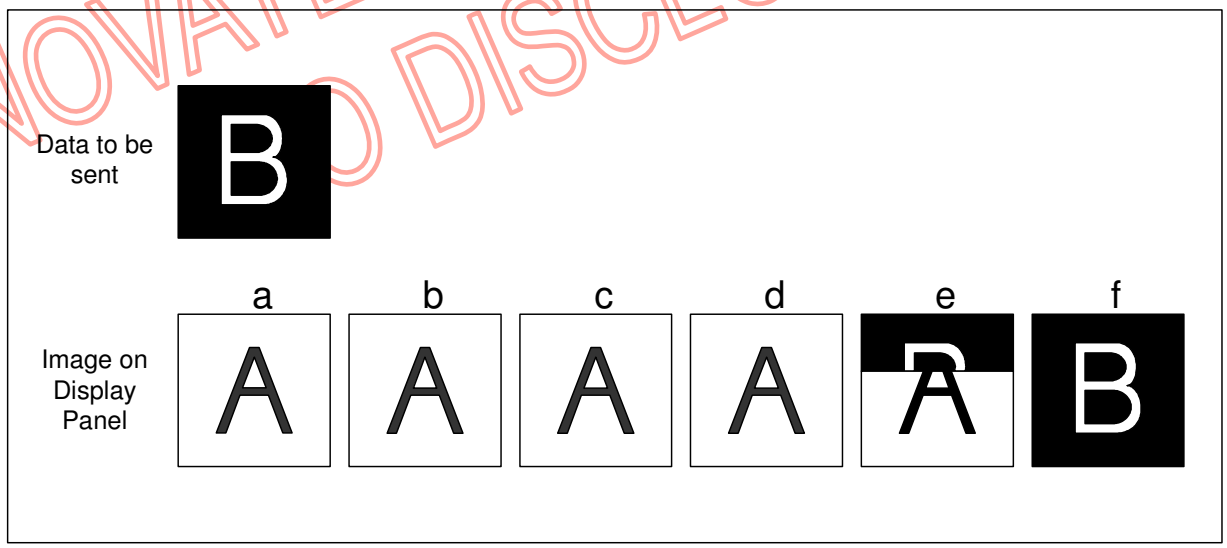
Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:



5.8.1.4 EXAMPLE 2: MPU WRITE IS SLOWER THAN PANEL READ.



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



5.9 Checksum

The display module consists of two 8-bit checksum registers, which are used checksum calculations for “User Command Set” area registers (includes the frame memory), on the display module.

One of the checksum registers is “First Checksum” (FCS) and another is “Continue Checksum” (CCS).

These register values are set to 00h as an initial value when there is started to calculate a new checksum.

The display module is starting to calculate the new checksum after there is a write access on “User Command Set” area registers. This means that read commands are not used as a calculation starting trigger in this case.

The checksum calculation is always interrupted, when there is a new write access on Nokia area registers. The checksum calculation is also started from the beginning.

The result of the first finished checksum calculation is stored on the FCS register, which value is kept until there is the new write access on “User Command Set” area registers and the new checksum value is calculated in the first time again.

The maximum time, when the FCS is readable, is 150ms after there is the last write access on “User Command Set” area registers.

The checksum calculation is continuing after the finished first checksum calculation where the FCS has gotten the checksum value. These new checksum values are always stored on CCS register (Old value is replaced a new one) after the last Nokia area register has been calculated to the checksum.

The maximum time, when the CCS is readable in the first time, is 300ms after there is the last write access on “User Command Set” area registers.

There is always updated a checksum comparison bit (See section: “Read Display Self-Diagnostic Result (0Fh)” and bit D0) when there is compared FCS and CCS checksums after a new checksum value is stored on CCS.

The maximum time, when the comparison has been done between FCS and CCS in the first time, is 300ms then the comparison has been done in every 150ms (this is maximum time).

User can read FCS, CCS and Comparison bit D0 values. See section: “Read First Checksum (AAh)”, “Read Continue Checksum (AFh)” and ”Read Display Self-Diagnostic Result (0Fh)”.

There can be an overflow during a checksum calculation. These overflow bits are not needed to store anywhere. This means that these overflow bits can be ignored by the display module.

An example of the checksum calculation:
- Register Values: A1h, 12h, 81h, DEh, F2h
- Calculated Value: 304h (= A1h + 12h + 81h + DEh + F2h)
- Ignored Bits: 3h
- Stored Checksum: 04h

This checksum calculation function is only running in “Sleep Out” mode and it is stopped in “Sleep In” mode.

Table 5.9.1 Checksum Sequence

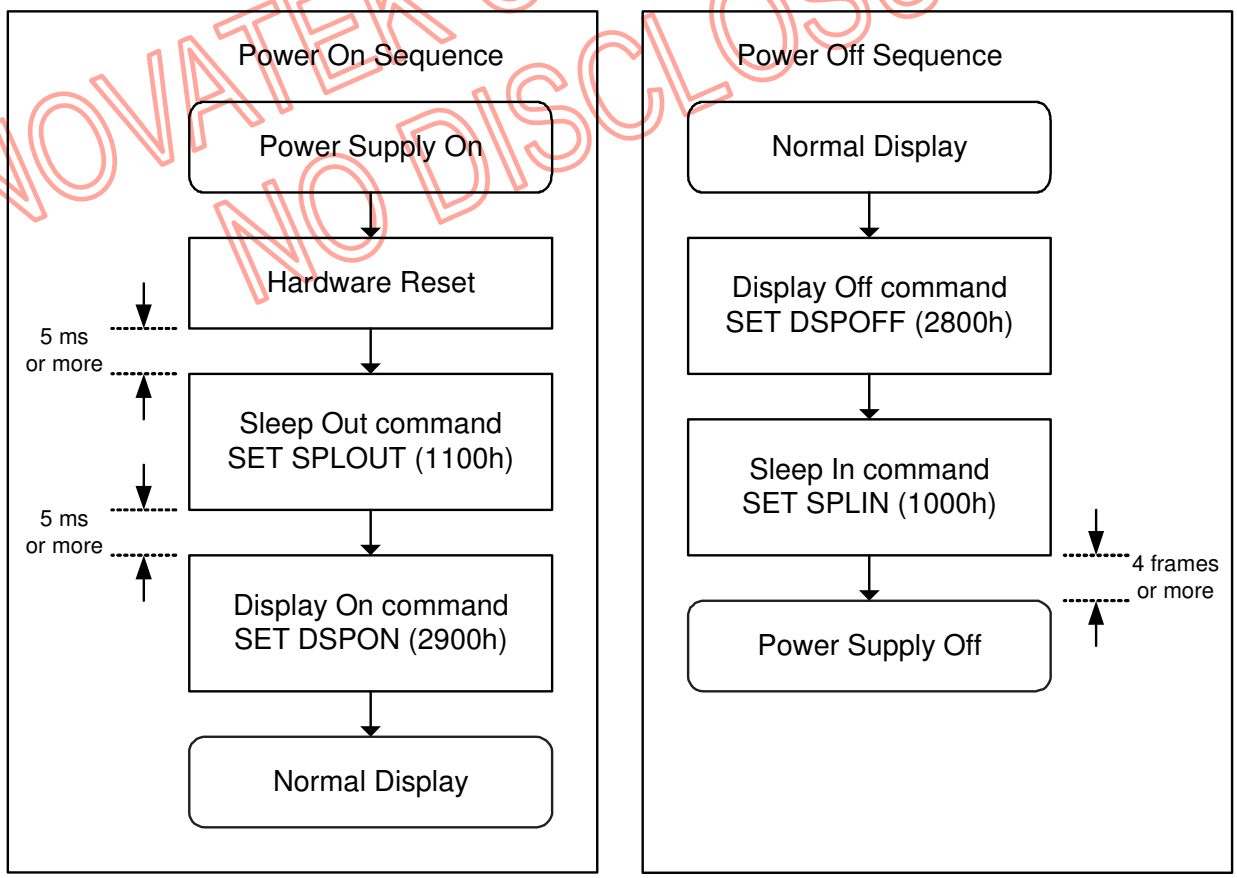
Step Note1	Time Note2	Action	Temporary Register	First Checksum Register (FCS)	Continue Checksum Register (CCS)	Comment
1	0	Initialization	Set to 00h	Set to 00h	Set to 00h	The last write action on “User Command Set” area registers => FCS an CCS registers are initialized
2	0 | 150ms	Continue sum of “User Command Set” area registers	Counting	-	-	The first register counting is running
3	150ms	Stores sum of registers on FCS register	Set to 00h after value is moved to FCS register	Stores sum of “User Command Set” area registers on FCS register	-	The result of the first register counting is stored on FCS register. The result of the FCS is available to the MPU
4	150ms | 300ms	Continue sum of “User Command Set” area registers	Counting	-	-	The second register counting is running
5	300ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
6	300ms | 450ms	Continue sum of “User Command Set” area registers	Counting	-	-	The third register counting is running
7	450ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
8	450 | 600ms	Continue sum of “User Command Set” area registers	Counting	-	-	The fourth register counting is running
9	600ms	1) Stores sum of registers on CCS register 2) Compares stored FCS and CCS value	Set to 00h after value is moved to CCS register	-	Stores sum of “User Command Set” area registers on CCS register	The result of the comparison is stored on separated registers, which can read separated read commands. The result of the CCS and comparison result are available to the MPU
10	etc	-	-	-	-	Same sequence continue e.g. step 4 and 5

5.10 Power On/Off Sequence

VDDI and VDD (VDDA) can be applied in any order.
VDD (VDDA) and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD (VDDA) and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA) can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.
Notes:

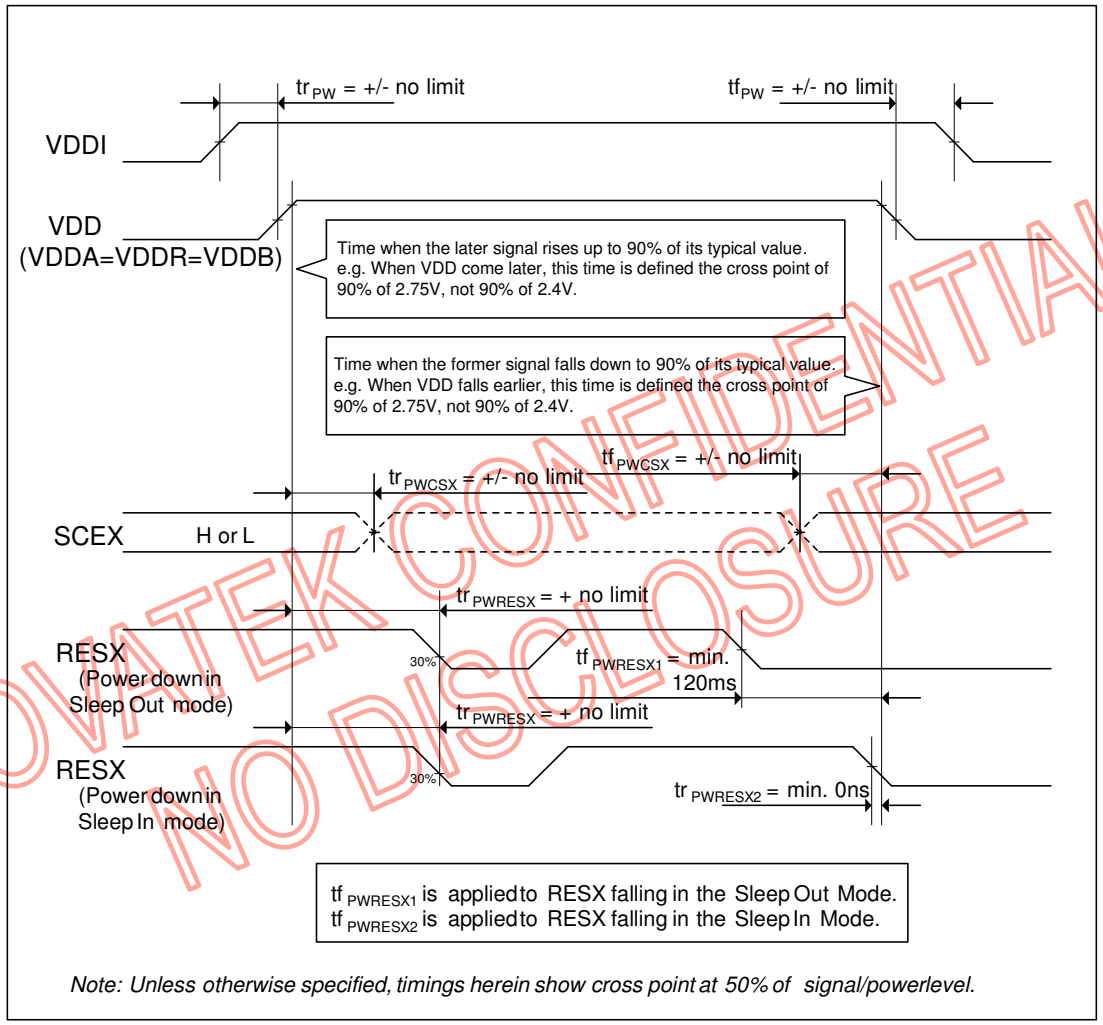
1. *There will be no damage to the display module if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.10.1 and 5.10.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *There is not a limit for Rise/Fall time on VDDI and VDD (VDDA).*
6. *The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).*

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



5.10.1 Case 1 – RESX line is held High or Unstable by Host at Power On

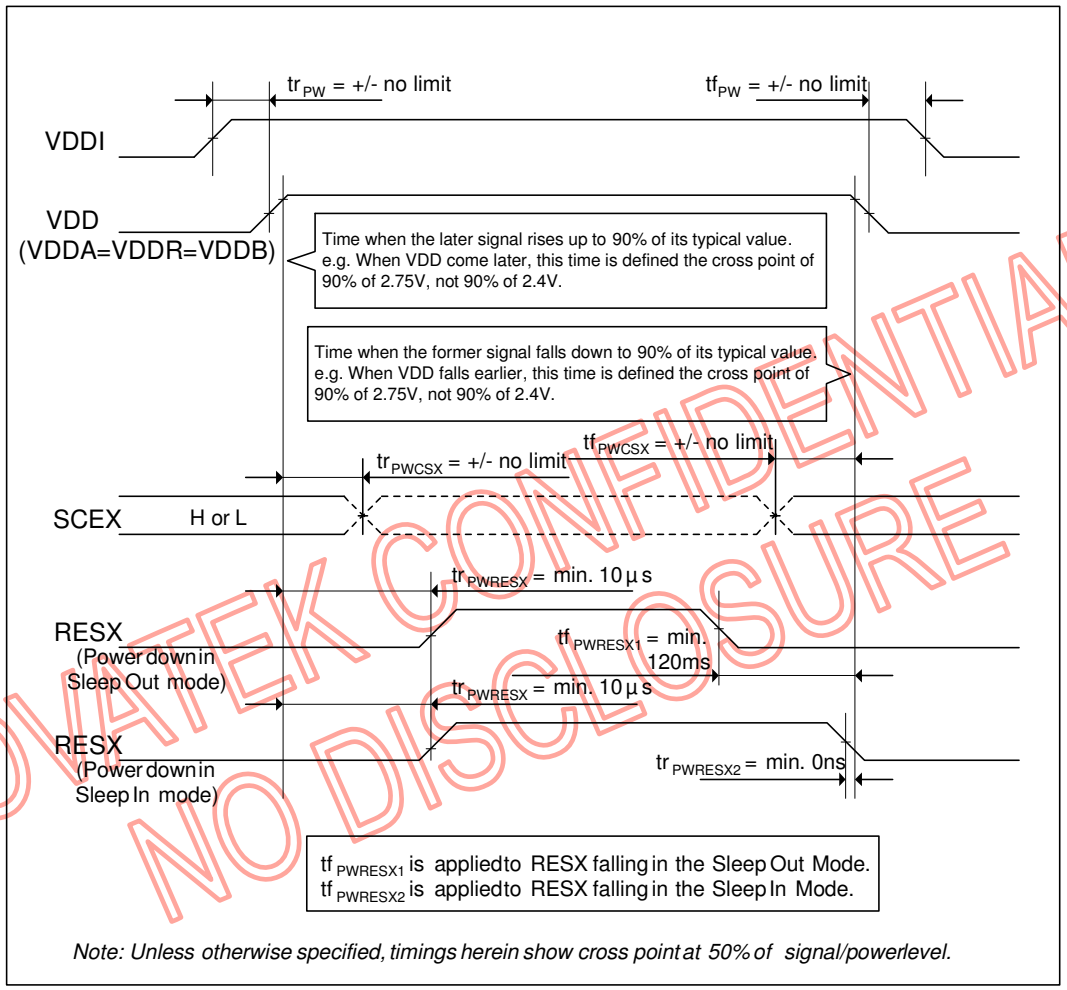
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/powerlevel.

5.10.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.



5.10.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.11 Power Level Modes

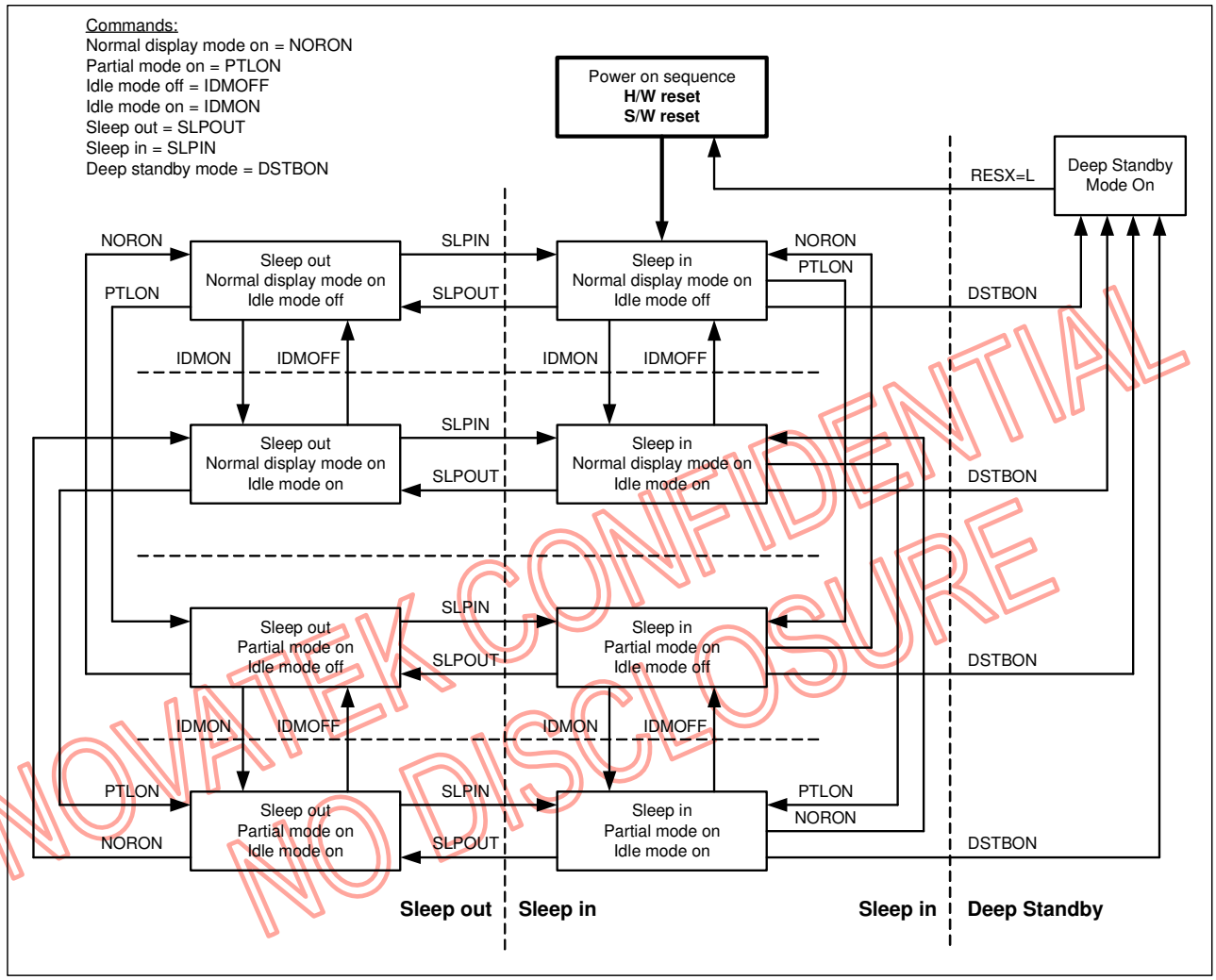
5.11.1 Definition

7 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 16.7M colors.
2. Partial Mode On, Idle Mode Off, Sleep Out
   In this mode, part of the display is used with maximum 16.7M colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.
6. Deep Standby Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory is random.
7. Power Off Mode
   In this mode, VDDI and VDDA/VDDR/VDDB are removed.

NOTE: Transition between mode 1~5 is controllable by MPU commands. Mode 6 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 7 is entered only when both power supplies for I/O and analog circuits are removed.

5.11.2 Power Level Mode Flow Chart



NOTES:

1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.

2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

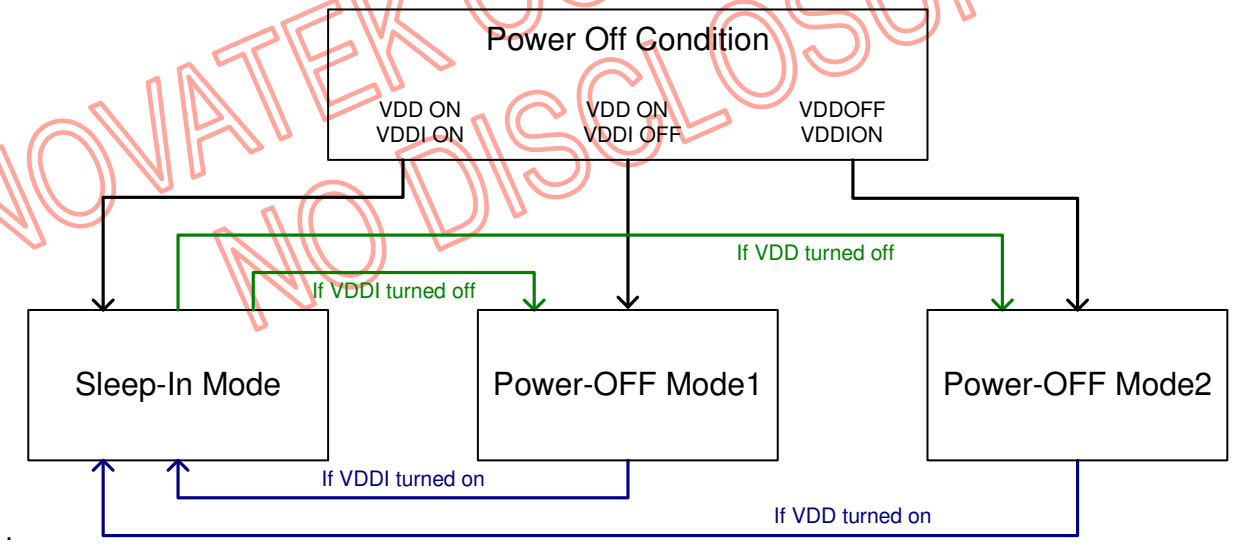
The following table represents the SRAM and Registers its mode state.

Mode	SRAM	Register	Control	
			Enter	Exit
Sleep in mode 1 (RAMKP = 1)	Keep	Keep	Command	
Sleep in mode 2 (RAMKP = 0)	Loss	Keep	Command	
Deep-standby mode	Loss	Loss	Command	Reset pin
Reset=L	Loss	Keep (Default Value)	Reset (H/W)	

The condition for irregular power off mode is shown below.

Power Off Mode	VDD	VDDI	RESX	I/O
Mode 1	ON	OFF	High or Low	Low
Mode 2	OFF	ON	High or Low	Low

Note: VDD means VDDA, VDDR, VDDB and VDDAM



5.12 Reset function

5.12.1 Register Default Value

Table 5.12.1 Default Values for User Command Set

Item		After Power On	After Hardware Reset	After Software Reset
RDNUMPE (05h)		00h	00h	00h
RDDPM (0Ah)		08h	08h	08h
RDDMADCTR (0Bh)		00h	00h	00h
RDDCOLMOD (0Ch)		07h	07h	07h
RDDIM (0Dh)		00h	00h	00h
RDDSM (0Eh)		00h	00h	00h
RDDSDR (0Fh)		00h	00h	00h
Sleep In/Out (10h/11h)		In	In	In
Partial/Normal Display (12h/13h)		Normal	Normal	Normal
Display Inversion On/Off (21h/20h)		Off	Off	Off
All Pixel On/Off (23h/22h)		Off	Off	Off
Gamma setting (26h)		01h (GC0)	01h (GC0)	01h (GC0)
Display On/Off (29h/28h)		Off	Off	Off
Column: Start Address (XS, 2Ah)		0000h	0000h	0000h
Column: End Address (XE, 2Ah)	CGM[7:0]=“70h” (480x864)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]=“6Bh” (480x854)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]=“50h” (480x800)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]=“28h” (480x720)	01DFh (479d)	01DFh (479d)	01DFh (479d)
	CGM[7:0]=“00h” (480x640)	01DFh (479d)	01DFh (479d)	01DFh (479d)
Row: Start Address (YS, 2Bh)		0000h	0000h	0000h
Row: End Address (YE, 2Bh)	CGM[7:0]=“70h” (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)
	CGM[7:0]=“6Bh” (480x854)	0355h (853d)	0355h (853d)	0355h (853d)
	CGM[7:0]=“50h” (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)
	CGM[7:0]=“28h” (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)
	CGM[7:0]=“00h” (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)
Frame memory (2Ch, 2Eh, 3Ch, 3Eh)		Random	Random	Random
Partial: Start Address (PSL, 30h)		0000h	0000h	0000h
Partial: End Address (PEL, 30h)	CGM[7:0]=“70h” (480x864)	035Fh (863d)	035Fh (863d)	035Fh (863d)
	CGM[7:0]=“6Bh” (480x854)	0355h (853d)	0355h (853d)	0355h (853d)
	CGM[7:0]=“50h” (480x800)	031Fh (799d)	031Fh (799d)	031Fh (799d)
	CGM[7:0]=“28h” (480x720)	02CFh (719d)	02CFh (719d)	02CFh (719d)
	CGM[7:0]=“00h” (480x640)	027Fh (639d)	027Fh (639d)	027Fh (639d)
Tearing: On/Off (35h/34h)		Off	Off	Off

Table 5.12.1 Default Values for User Command Set (Continuous)

Item		After Power On	After Hardware Reset	After Software Reset
Memory Data Access Control (36h) (MY/MX/MV/ML/RGB/MH/RSMX/RSMY)		00h	00h	00h
Idle Mode On/Off (38h/39h)		Off	Off	Off
Interface Pixel Color Format (3Ah)		77h	77h	77h
Set Tearing Effect Scan Line (44h)		0000h	0000h	0000h
Get Scan Line (45h)		N/A	N/A	N/A
DSTB mode (4Fh)		00h	00h	00h
Profile Value for Display (50h)		All values are FFh	All values are FFh	All values are FFh
Display Brightness (51h, 52h)		00h	00h	00h
CTRL Display (53h, 54h)		00h	00h	00h
CABC Control (55h, 56h)		00h	00h	00h
Write Hysteresis (57h)		All values are FFh	All values are FFh	All values are FFh
Write Gamma Setting (58h)		All values are 11h	All values are 11h	All values are 11h
RDFSVM (5Ah)		00h	00h	00h
RDFSVL (5Bh)		00h	00h	00h
RDMFFSVM (5Ch)		00h	00h	00h
RDMFFSVL (5Dh)		00h	00h	00h
RDLSCCM (65h, 66h)		80h	80h	80h
RDLSCCL (65h, 67h)		00h	00h	00h
Black/White Color Characteristics (70h~74h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
Red/Green Color Characteristics (75h~79h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
Blue/AColor Color Characteristics (7Ah~7Eh)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
DDB Start/Continue (A1h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
DDB Continue (A8h)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	00h	00h	00h
First/Continue Checksum (AAh, AFh)		00h	00h	00h
ID1 (DAh) ID2 (DBh) ID3 (DCh)	After MTP	MTP Value	MTP Value	MTP Value
	Before MTP	ID1 = ”00h” ID2 = “80h” ID3 = “00h”	ID1 = ”00h” ID2 = “80h” ID3 = “00h”	ID1 = ”00h” ID2 = “80h” ID3 = “00h”

5.12.2 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins		After Power On	After Hardware Reset	After Software Reset
HSSI_DATA0_P, HSSI_DATA0_N		High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
TE		VSSI	VSSI	VSSI
SDO	Using SPI	VDDI	VDDI	VDDI
	Not using SPI	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
Source Driver Output		High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
GOUT1~GOUT32		AVSS	AVSS	AVSS

NOTE: There will be no output from TE, SDO, D23-D0, HSSI_DATA0_P/N and HSSI_DATA1_P/N during Power On/Off sequence, H/W Reset and S/W Reset

5.12.3 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 5.10	Input Valid	Input Valid	Input Valid	See Section 5.10
CSX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
D/CX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
WRX (SCL / I2C_SDA)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
RDX	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
D23 to D0	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
SDI (I2C_SCL)	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
VS	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
PCLK	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
DE	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_CLK_P, HSSI_CLK_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA0_P, HSSI_DATA0_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA1_P, HSSI_DATA1_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid

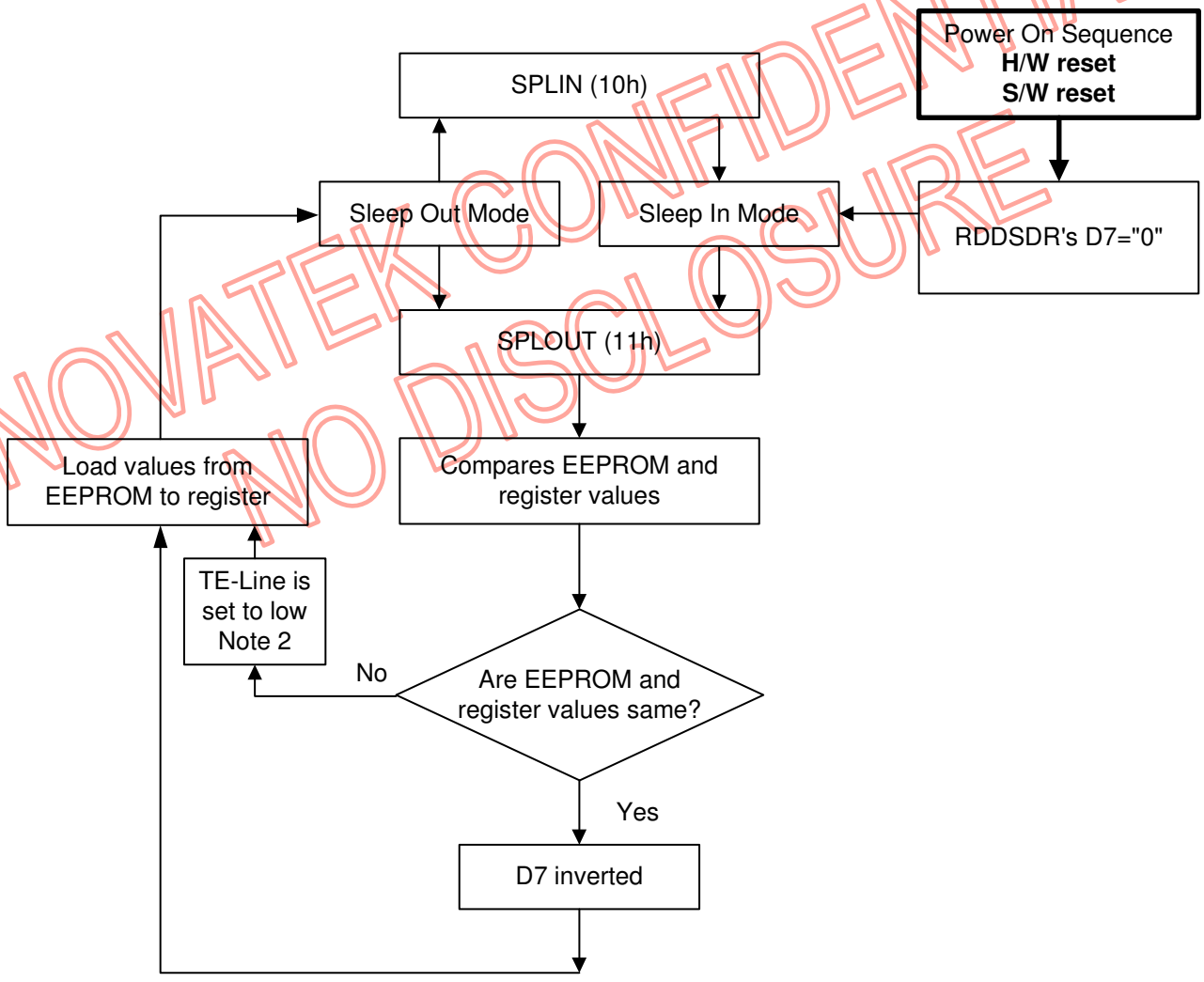
5.13 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.13.1 Register loading Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of these commands is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is following:



NOTES:

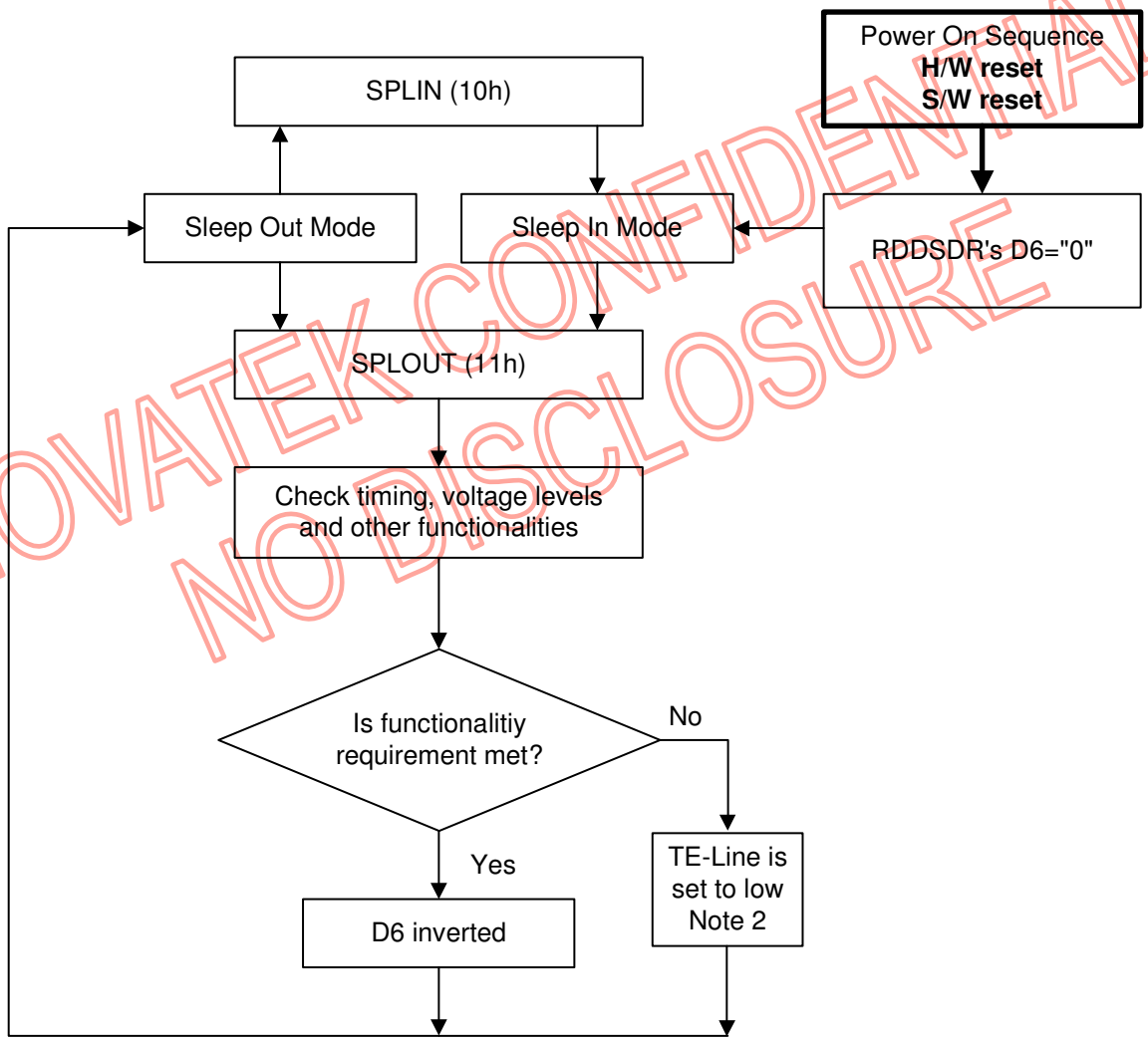
1. *There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DCh), by the display module.*
2. *This information is only used if TE line is used.*

5.13.2 Functionality Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of these commands is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The flow chart for this internal function is following:



NOTES:

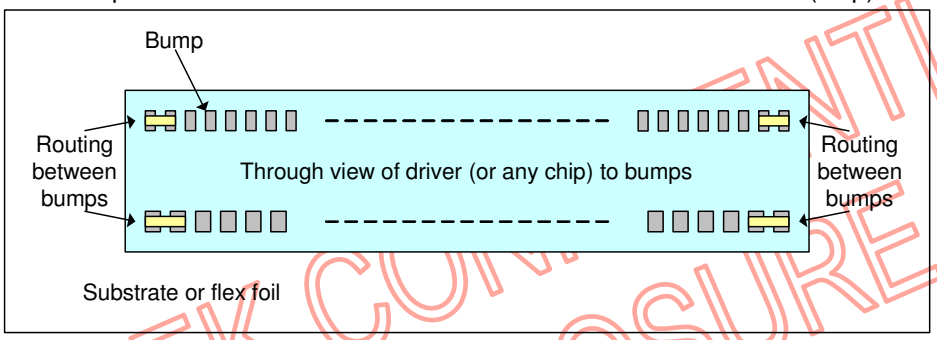
1. *There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.*
2. *This information is only used if TE line is used.*

5.13.3 Chip Attachment Detection

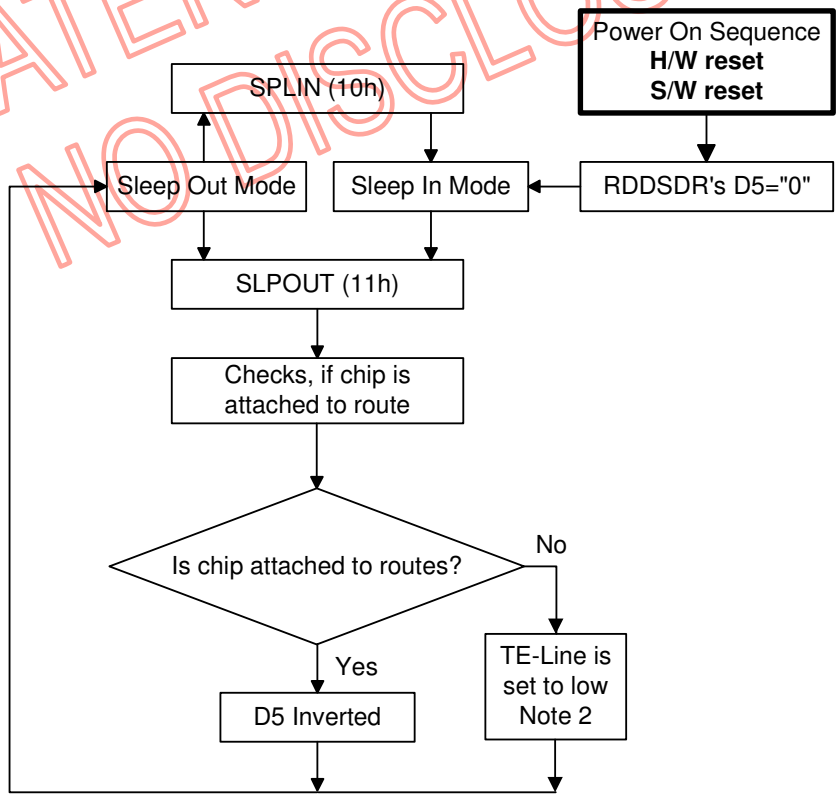
Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if a chip or chips (e.g. driver, etc.) of the display module is/are attached to the circuit route of a flex foil or display glass ITO.

There is inverted (= increased by 1) a bit, which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D5), if the chip or chips is/are attached to the circuit route of the flex or display glass. If this chip is or those chips are not attached to the circuit route of the flex or display glass, this bit (D5) is not inverted (= not increased by 1) and the used TE-line ie set to low (Registers, what are set by “Tearing Effect Line On (35h)” command, are keeping their current values) when it can be reactivated by “Tearing Effect Line On (35h)” command.

The following figure is for reference purposes; how this chip attachment can be implemented e.g. there are connected together 2 bumps via route of ITO or the flex foil on 4 corners of the driver (chip).



The flow chart for this internal function is following:



NOTE: This information is only used if TE line is used.

5.14 Display Panel Color Characteristics

Color characteristics of the display panel are stored on the display module that they can be read via the used interface by the engine what is using this display panel color characteristics information to adjust a color information of the image frame, what is on the engine, to match a wanted color outlook of the image on the display panel.

Used color characteristics can share 2 categories: Mandatory and Optional. The mandatory color characteristics are Black, White, Red, Green and Blue. The optional color characteristics is used if it is needed and it is called as A color (e.g. Cyan). The bits of the A color are set to '0's they are not used on the display module.

A read color characteristic value is based on 10 bit floating value where the MSB is 9^{th} bit and the LSB is 0^{th} bit. All power values of the bits are listed below:
- Bit 9: 2-1 = 0.5,
- Bit 8: 2-2 = 0.25,
- Bit 7: 2-3 = 0.125,
- Bit 6: 2-4 = 0.0625,
- Bit 5: 2-5 = 0.03125,
- Bit 4: 2-6 = 0.015625,
- Bit 3: 2-7 = 0.007813,
- Bit 2: 2-8 = 0.003906,
- Bit 1: 2-9 = 0.001953,
- Bit 0: 2-10 = 0.000977.

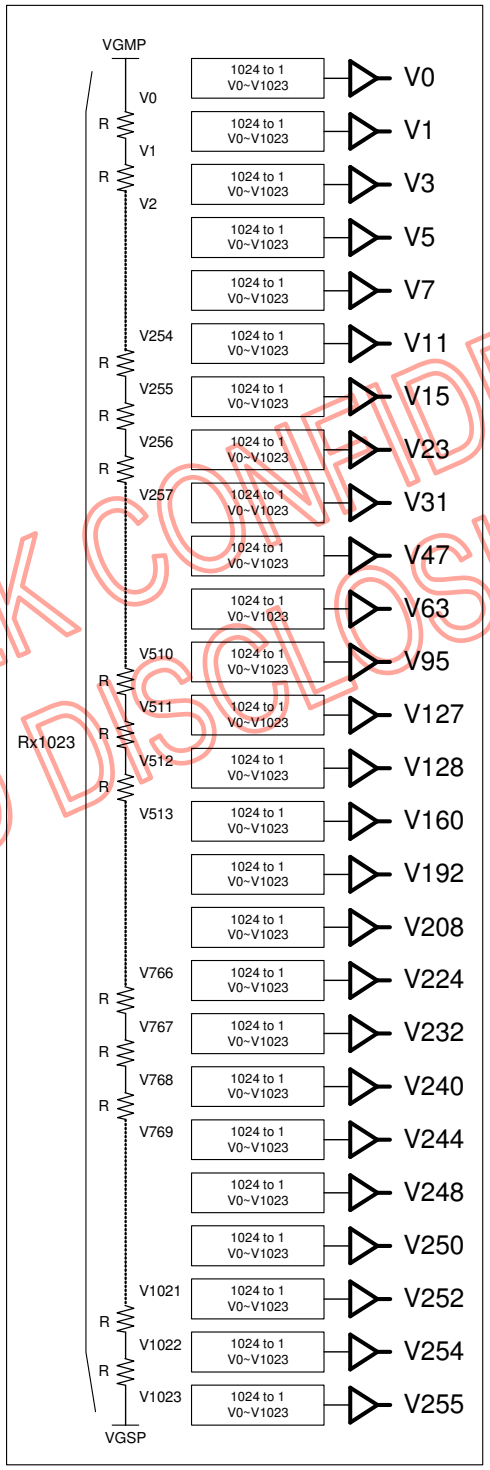
The wanted value is an approximation in the most of the cases when there is used binary numbers. Therefore, there is used the nearest value what can get e.g. Rx can be:
- Actual value: 0.6400, Stored value Rx[9:0] = 10 1000 1111b = 0.6396,
- Actual value: 0.3300, Stored value Rx[9:0] = 01 0101 0010b = 0.3301,
- Actual value: 0.3000, Stored value Rx[9:0] = 01 0011 0011b = 0.2998,
- Actual value: 0.6000, Stored value Rx[9:0] = 10 0110 0101b = 0.5986,
- Actual value: 0.1500, Stored value Rx[9:0] = 00 1001 1010b = 0.1504,
- Actual value: 0.0600, Stored value Rx[9:0] = 00 0011 1101b = 0.0596,
- Actual value: 0.3127, Stored value Rx[9:0] = 01 0100 0000b = 0.3125,
- Actual value: 0.3290, Stored value Rx[9:0] = 01 0101 0001b = 0.3291.

The value 0.6396 has calculated as follows:
- Binary value: 10 1000 1111b
- Formula: Rx[9]x0.5+Rx[8]x0.25+Rx[7]x0.125+Rx[6]x0.0625+Rx[5]x0.03125+Rx[4]x0.015625+ Rx[3]x0.007813+Rx[2]x0.003906+Rx[1]x0.001953+R[0]x0.000977
- Use: 1x0.5+0x0.25+1x0.125+0x0.0625+0x0.03125+0x0.015625+1x0.007813+1x0.003906+ 1x0.001953+1x0.000977

See also sections:
"Read Black/White Low Bits (70h)", "Read Bkx (71h)", "Read Bky (72h)", "Read Wx (73h)", "Read Wy (74h)", "Read Red/Green Low bits (75h)", "Read Rx (76h)", "Read Ry (77h)", "Read Gx (78h)", "Read Gy (79h)", "Read Blue/AColor Low Bits (7Ah)", "Read Bx (7Bh)", "Read By (7Ch)", "Read Ax (7Dh)", "Read Ay (7Eh)".

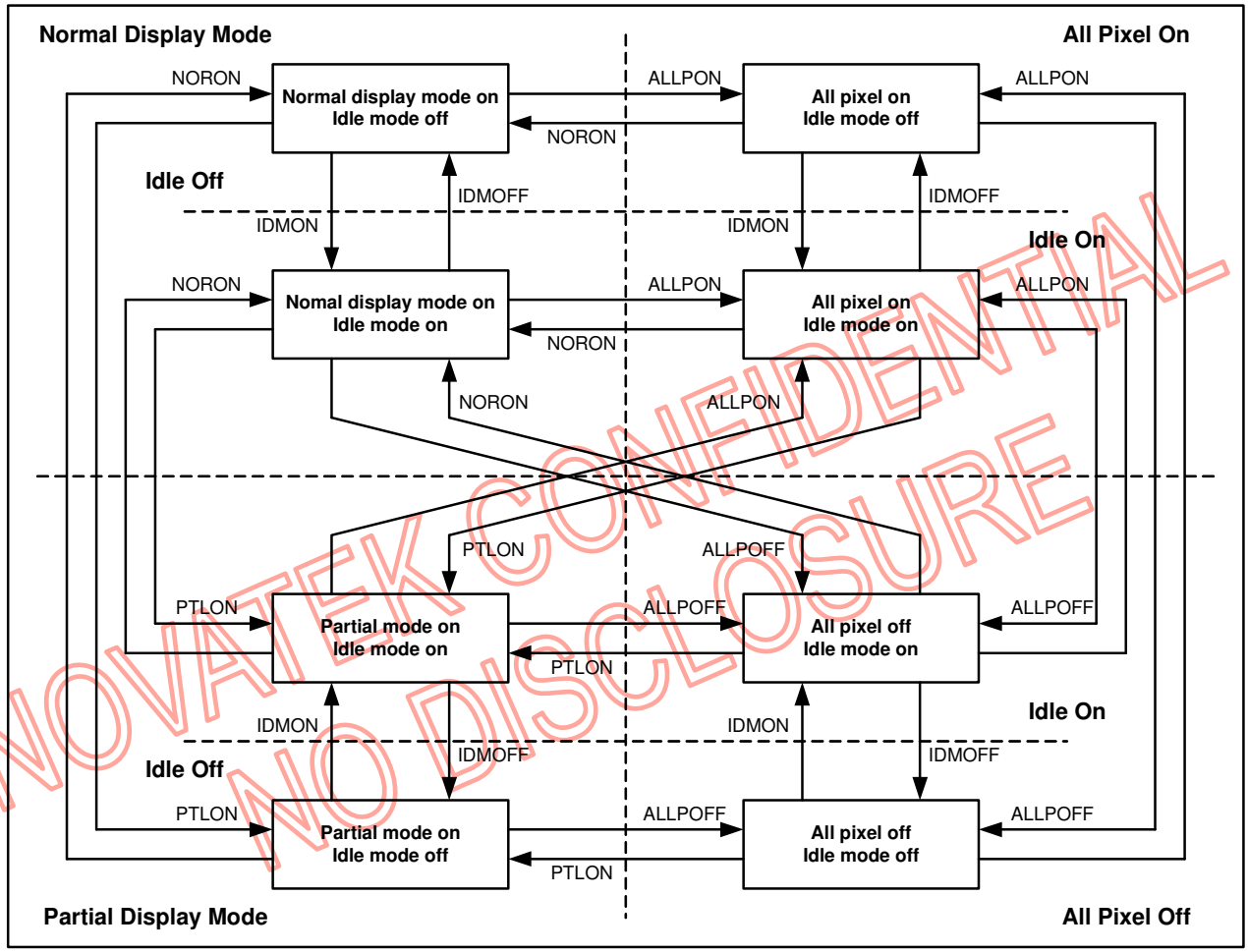
5.15 Gamma Function

The structure of grayscale amplifier is shown as below. The 26 voltage levels between VGMP and VGSP are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.



5.16 Basic Display Mode

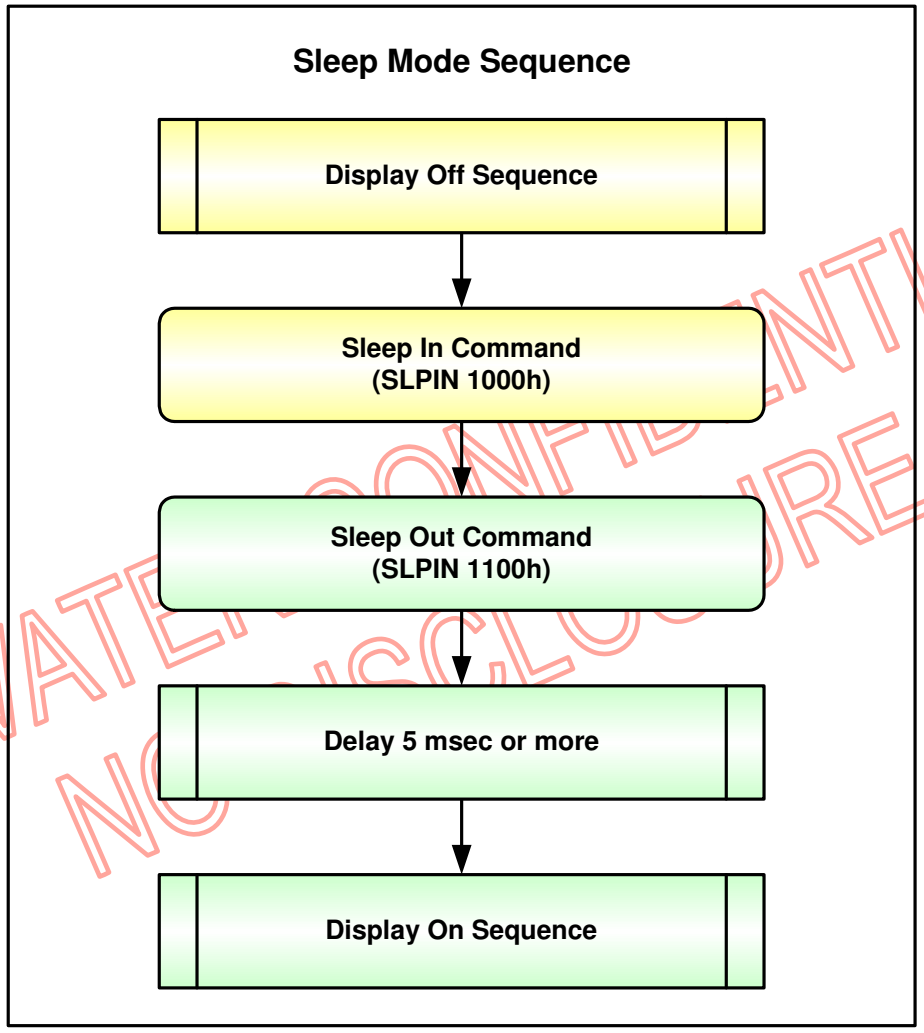
The NT35510 has some basic operation modes which are Normal Display Mode, Partial Display Mode, Idle Mode, All Pixel On and All pixel Off for panel display. User can change these display modes for each other is illustrated below.



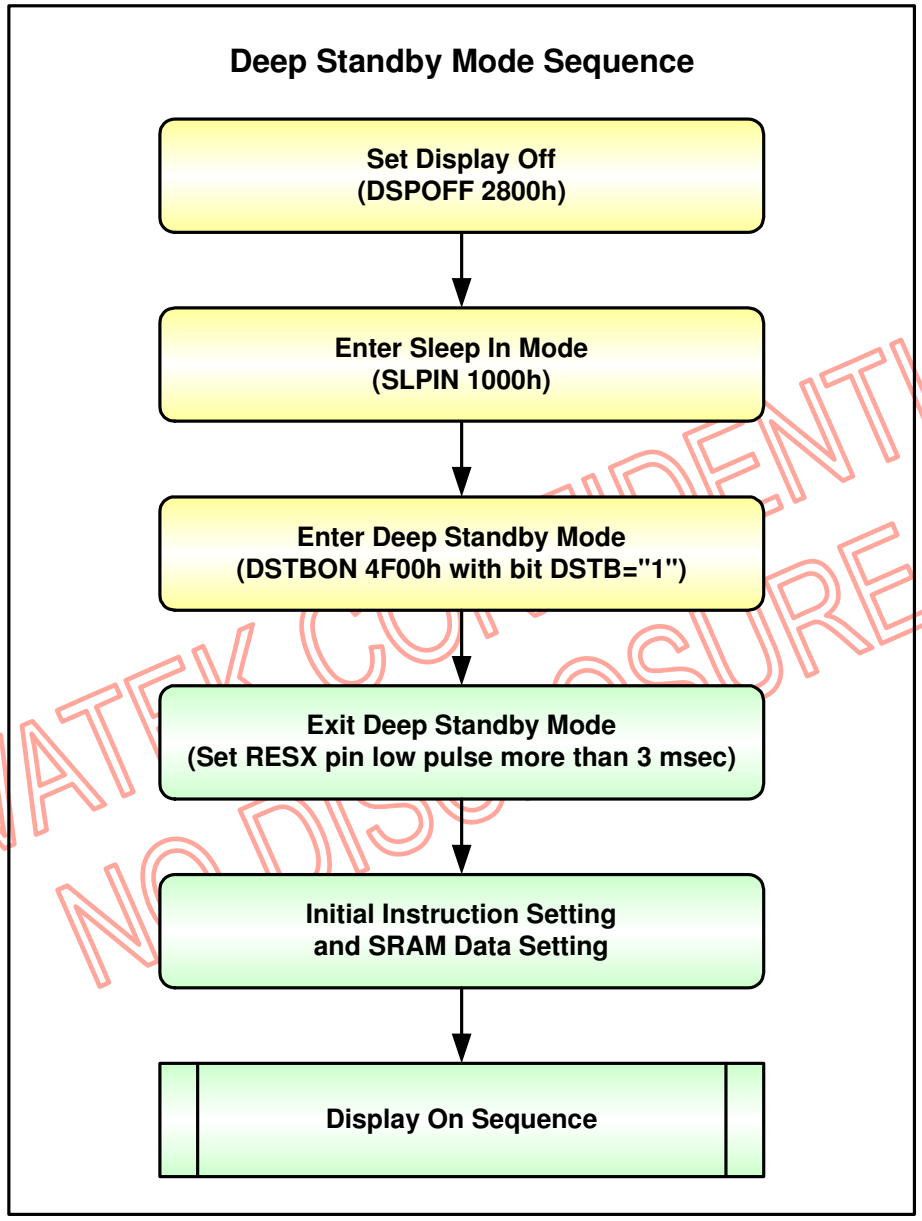
5.17 Instruction Setting Sequence

When setting instruction to the NT35510, the sequences shown in below figures must be followed to complete the instruction setting.

5.17.1 Sleep In/Out Sequence



5.17.2 Deep Standby Mode Enter/Exit Sequence



5.18 Instruction Setup Flow

5.18.1 Initializing with the Built-in Power Supply Circuits

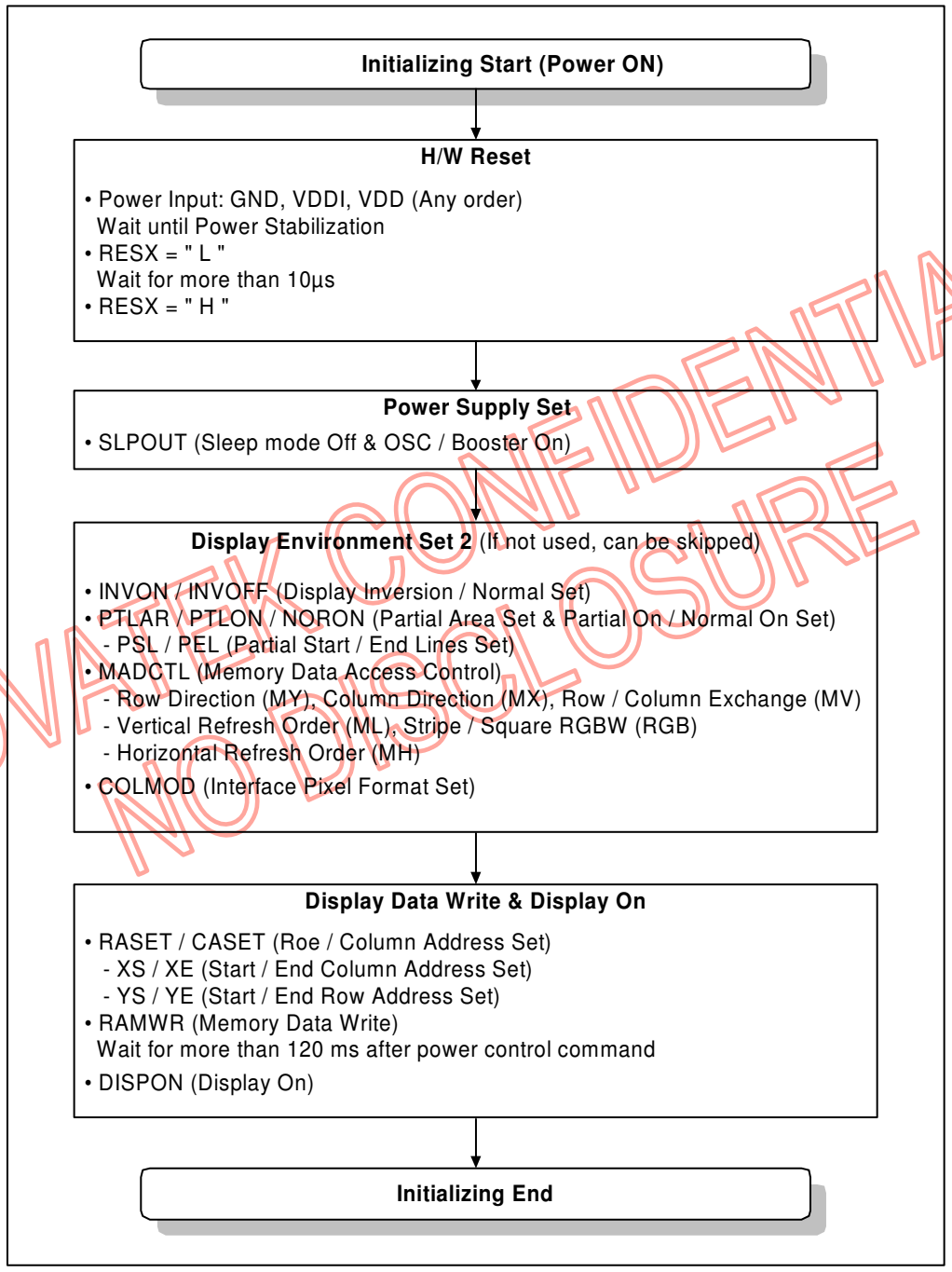


Fig. 5.18.1 Initializing with the built-in power supply circuit

The initializing sequence does not have any effect on the display. The display is in its normal background color during the initializing.

5.18.2 Power OFF Sequence

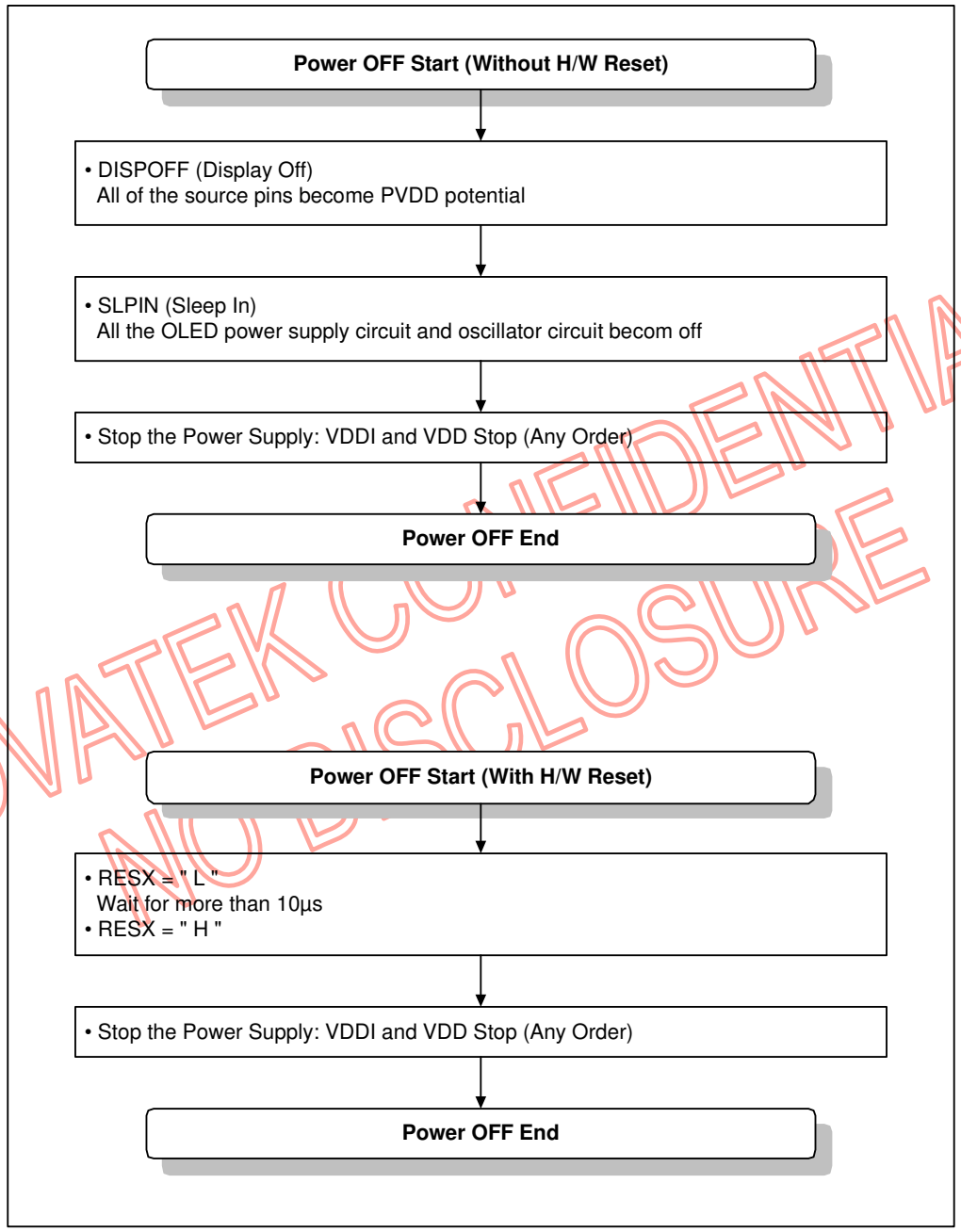
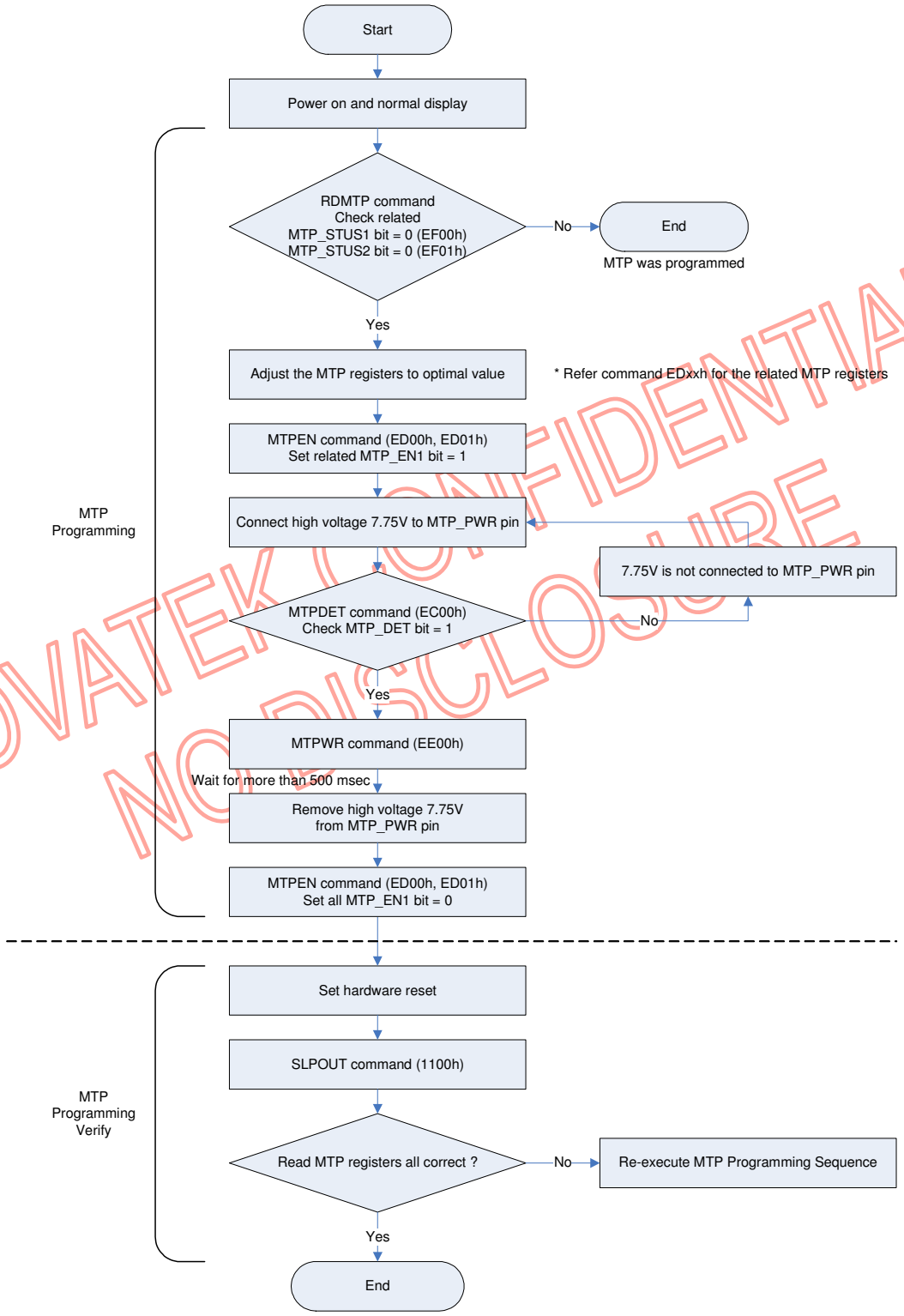


Fig. 5.18.2 Power off sequence

5.19 MTP Write Sequence



Note: The multi-times MTP must be programmed from the 1st time.
(ID1/2/3, VGMP/VGSP, VGMN/VGSN, VCOM, Gamma 2.2, VGMP/VGSP LUT)

5.20 Column, 1-Dot, 2-Dot, 3-Dot and 4-Dot Inversion (VCOM DC Drive)

The NT35510, in addition to the frame-inversion liquid crystal drive, supports the column, 1–dot, 2-dot, 3-dot and 4-dot inversion driving methods to invert the polarity of liquid crystal. The column, 1–dot, 2-dot, 3-dot and 4-dot inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

6 COMMAND DESCRIPTIONS

6.1 User Command Set

Table 6.1.1 User Command Set

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Dir	W	00h	0000h	No Argument (0000h in MDDI I/F)									No Operation
SWRESET	Cnd1	W	01h	0100h	No Argument (0000h in MDDI I/F)									Software reset
RDDID	Dir	R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID
				0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
				0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	
RDNUMPE	Dir	R	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Errors on DSI only
RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode
RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTR
RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Pixel Format
RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode
RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Signal Mode
RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result
SLPIN	DVS	W	10h	1000h	No Argument (0000h in MDDI I/F)									Sleep in & booster off
SLPOUT	Dir	W	11h	1100h	No Argument (0000h in MDDI I/F)									Sleep out & booster on
PTLON	DVS	W	12h	1200h	No Argument (0000h in MDDI I/F)									Partial mode on
NORON	DVS	W	13h	1300h	No Argument (0000h in MDDI I/F)									Partial off (Normal)
INVOFF	DVS	W	20h	2000h	No Argument (0000h in MDDI I/F)									Display inversion off (normal)
INVON	DVS	W	21h	2100h	No Argument (0000h in MDDI I/F)									Display inversion on
ALLPOFF	DVS	W	22h	2200h	No Argument (0000h in MDDI I/F)									All pixel off (black)
ALLPON	DVS	W	23h	2300h	No Argument (0000h in MDDI I/F)									All pixel on (white)
GAMSET	DVS	W	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select
DISPOFF	DVS	W	28h	2800h	No Argument (0000h in MDDI I/F)									Display off
DISPON	DVS	W	29h	2900h	No Argument (0000h in MDDI I/F)									Display on
CASET	Dir	W	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8	Column address set XS[15:0]: column start address XE[15:0]: column end address
				2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
				2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8	
				2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
RASET	Dir	W	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8	Row address set YS[15:0]: row start address YE[15:0]: row end address
				2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
				2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8	
				2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
RAMWR	Dir	W	2Ch	X	X	D7	D6	D5	D4	D3	D2	D1	D0	Memory write
RAMRD	Dir	R	2Eh	2E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read
PTLAR	DVS	W	30h	3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8	Partial start/end address set PSL[15:0]: partial start address PEL[15:0]: partial end address
				3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0	
				3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8	
				3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0	
TEOFF	DVS	W	34h	3400h	No Argument (0000h in MDDI I/F)									Tearing effect line off
TEON	DVS	W	35h	3500h	00h	-	-	-	-	-	-	-	M	Tearing effect mode set & on
MADCTL	Cnd2	W	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY	Memory data access control
IDMOFF	DVS	W	38h	3800h	No Argument (0000h in MDDI I/F)									Idle mode off
IDMON	DVS	W	39h	3900h	No Argument (0000h in MDDI I/F)									Idle mode on

Table 6.1.1 User Command Set (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	Dir	W	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format
RAMWRC	Dir	W	3Ch	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory write Continue
RAMRDC	Dir	R	3Eh	3C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Memory read Continue
STESL	DVS	W	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line
				4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
GSL	Dir	R	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line
				4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0	
DSTBON	DVS	W	4Fh	4F00h	00h	0	0	0	0	0	0	0	DSTB	Deep standby mode on
WRPFD	DVS	W	50h	5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010	Write profile value for display
				5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020	
				:	:	:	:	:	:	:	:	:	:	
				500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150	
				500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160	
WRDISBV	DVS	W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness
RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value
WRCTRLD	DVS	W	53h	5300h	00h	0	0	BCTRL	A	DD	BL	DB	G	Write control display
RDCTRLD	Dir	R	54h	5400h	00h	0	0	BCTRL	A	DD	BL	DB	G	Read control display value
WRCABC	DVS	W	55h	5500h	00h	0	0	0	0	0	0	C1	C0	Write CABC mode
RDCABC	Dir	R	56h	5600h	00h	0	0	0	0	0	0	C1	C0	Read CABC mode
WRHYSTE	DVS	W	57h	5700h	00h	I017	I016	I015	I014	I013	I012	I011	I010	Write hysteresis
				5701h	00h	I027	I026	I025	I024	I023	I022	I021	I020	
				:	:	:	:	:	:	:	:	:	:	
				570Eh	00h	I157	I156	I155	I154	I153	I152	I151	I150	
				570Fh	00h	I167	I166	I165	I164	I163	I162	I161	I160	
				5710h	00h	D017	D016	D015	D014	D013	D012	D011	D010	
				5711h	00h	D027	D026	D025	D024	D023	D022	D021	D020	
				:	:	:	:	:	:	:	:	:	:	
				571Eh	00h	D157	D156	D155	D154	D153	D152	D151	D150	
				571Fh	00h	D167	D166	D165	D164	D163	D162	D161	D160	
WRGAMMSET	DVS	W	58h	5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010	Write gamma setting
				5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030	
				:	:	:	:	:	:	:	:	:	:	
				5806h	00h	G143	G142	G141	G140	G133	G132	G131	G130	
				5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150	
RDFSVM	Dir	R	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8	Read FS value MSBs
RDFSVL	Dir	R	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0	Read FS value LSBs
RDMFFSVM	Dir	R	5Ch	5C00h	00h	FFSV15	FFSV14	FFSV13	FFSV12	FFSV11	FFSV10	FFSV9	FFSV8	Read median filter FS value MSBs
RDMFFSVL	Dir	R	5Dh	5D00h	00h	FFSV7	FFSV6	FFSV5	FFSV4	FFSV3	FFSV2	FFSV1	FFSV0	Read median filter FS value LSBs
WRCABCMB	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness
RDCABCMB	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness

Table 6.1.1 User Command Set (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRLSCC	DVS	W	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Write light sensor compensation coefficient
				6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	
RDLSCCM	Dir	R	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	Read LSCC value MSBs
RDLSCCL	Dir	R	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	Read LSCC value LSBs
RDBWLB	Dir	R	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0	Read Black/White low bit
RDBkx	Dir	R	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2	Read Bkx
RDBky	Dir	R	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2	Read Bky
RDWx	Dir	R	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2	Read Wx
RDWy	Dir	R	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2	Read Wy
RDRGLB	Dir	R	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0	Read Red/Green low bit
RDRx	Dir	R	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Read Rx
RDRy	Dir	R	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2	Read Ry
RDGx	Dir	R	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2	Read Gx
RDGy	Dir	R	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2	Read Gy
RDBALB	Dir	R	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0	Read Blue/AColor low bit
RDBx	Dir	R	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2	Read Bx
RDBy	Dir	R	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2	Read By
RDAx	Dir	R	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2	Read Ax
RDAy	Dir	R	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2	Read Ay
RDDDBS	Dir	R	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB start
				A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
				A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A104h	00h	1	1	1	1	1	1	1	1	
RDDDBC	Dir	R	A8h	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB continue
				A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
				A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A804h	00h	1	1	1	1	1	1	1	1	
RDFCS	Dir	R	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	Read first checksum
RDCCS	Dir	R	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0	Read continue checksum
RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:

1. The following description is indicates the executing time of instructions.

<table>
<tr><th>No.</th><th>Symbol</th><th>Executing Time</th></tr>
<tr><td>1</td><td>Dir (Direct)</td><td>At the received a completed instruction and parameter</td></tr>
<tr><td>2</td><td>DVS (Display Vertical Sync.)</td><td>Synchronized with the next frame</td></tr>
<tr><td>3</td><td>DHS (Display Horizontal Sync.)</td><td>Synchronized with the next line</td></tr>
<tr><td>4</td><td>Cnd1 (By Conditional 1)</td><td><table><tr><th>State</th><th>Executing time</th></tr><tr><td>When Sleep In</td><td>Dir</td></tr><tr><td>Other</td><td>DHS</td></tr></table></td></tr>
<tr><td>5</td><td>Cnd2 (By Conditional 2)</td><td><table><tr><th>State</th><th>Executing time</th></tr><tr><td>B7, B6, B5</td><td>Dir</td></tr><tr><td>B4, B3, B2, B1, B0</td><td>DVS</td></tr></table></td></tr>
</table>

2. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "5.4 DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32 (In case of other interfaces, parameters of command 2A00h~2A03h are stored on relative registers while command 2A00h~2A03h are executed completely and same for command 2B00h~2B03h, 3000h~3003h and 4000h~4001h).

3. When using the commands without parameter (No Argument) in MDDI interface, a dummy parameter must be followed after command address. For example, command SPLOUT can be executed as 0x11 only in MIPI, MPU and SPI interfaces but should be executed as 0x1100 + 0x0000 in MDDI interface.

NOP (0000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NOP	Write	00h	0000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write, RAM data read, RAM data write continue or RAM data read continue as described in RAMWR (Memory Write), RAMRD (Memory Read), RAMWRC (Memory Write Continue) and RAMRDC (Memory Read Continue) and parameter write commands.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart	-

SWRESET: Software Reset (0100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SWRESET	Write	01h	0100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description)
The display is blank immediately.
Note: The Frame Memory content is kept or not by this command.

Restriction

It will be necessary to wait 5msec before sending new command following software reset.
The display module loads all display supplier's factory default values to the registers during this 5msec.
If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.
Software Reset command cannot be sent during Sleep Out sequence.

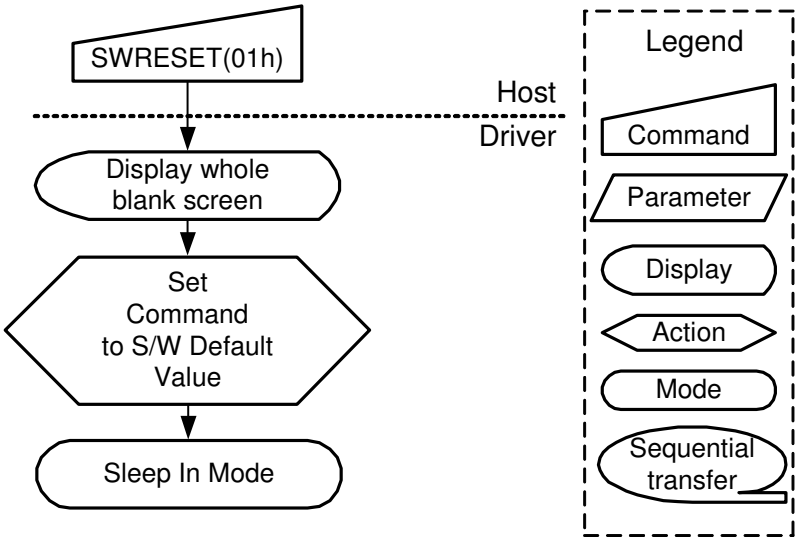
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



RDDID: Read Display ID (0400h~0402h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDID	Read	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
			0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
			0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

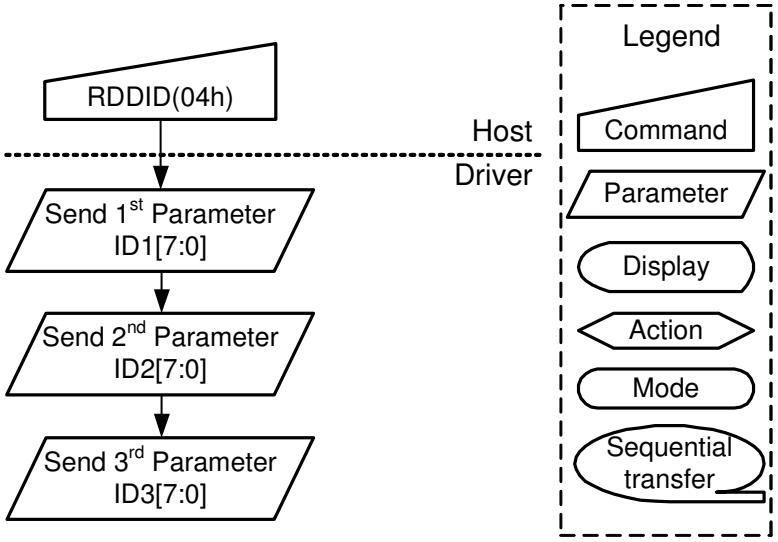
Description	This read byte returns 24-bit display identification information. The 1st parameter (ID1): the module's manufacture ID. The 2nd parameter (ID2): the module/driver version ID. The 3rd parameter (ID3): the module/driver ID. *Note: Commands RDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameter 1, 2, 3 of the command 04h, respectively.*
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Values	ID1=00h, ID2=80h, ID3=00h
S/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h
H/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h

Flow Chart



RDNUMED: Read Number of Errors on DSI (0500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDNUMED	Read	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0

NOTE: "-" Don't care

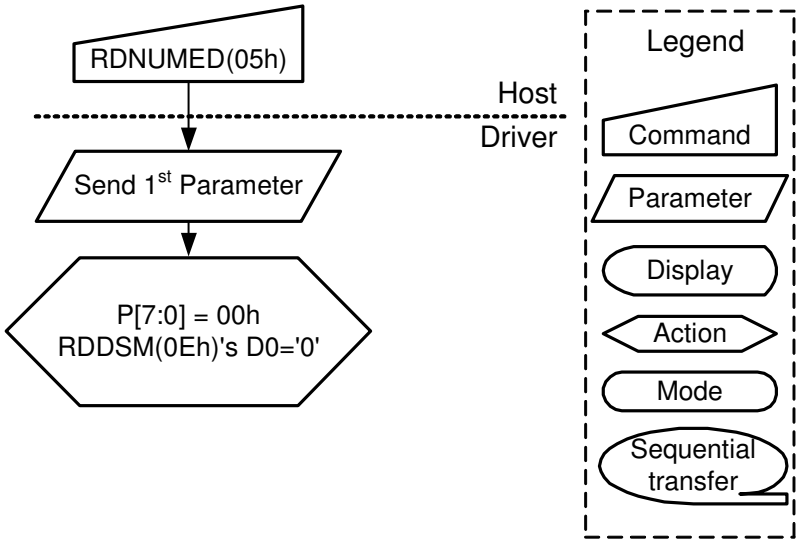
Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to "1" if there is overflow with P[6..0] bits. P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed). See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh. This command is used for MIPI DSI only. It is no function for others interface operation.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDPM: Read Display Power Mode (0A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDPM	Read	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1"=Booster On, "0"=Booster Off
D6	Idle Mode On/Off	"1"=Idle Mode On, "0"=Idle Mode Off
D5	Partial Mode On/Off	"1" = Partial Mode On, "0" = Partial Mode Off
D4	Sleep In/Out	"1" = Sleep Out Mode, "0" = Sleep In Mode
D3	Display Normal Mode On/Off	"1" = Display Normal On, "0" = Display Normal Off
D2	Display On/Off	"1" = Display is On, "0" = Display is Off
D1	Not Defined	Set to "0" (not used)
D0	Not Defined	Set to "0" (not used)

Restriction

-

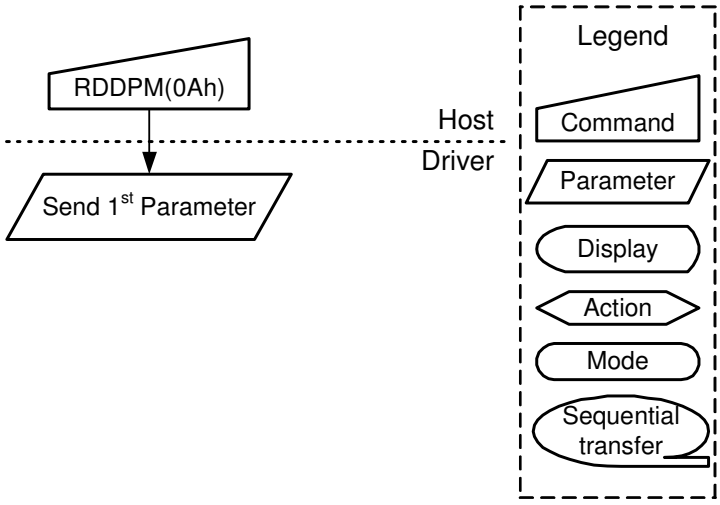
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



RDDMADCTL: Read Display MADCTL (0B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDMADCTL	Read	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Row Address Order (MY)	"0" = Increment , "1" = Decrement
D6	Column Address Order (MX)	"0" = Increment , "1" = Decrement
D5	Row/Column Exchange (MV)	"0"= Normal , "1"= Row/column exchange
D4	Vertical refresh Order (ML)	"0" = Increment , "1" = Decrement
D3	RGB-BGR Order	"0" = RGB color sequence "1" = BGR color sequence
D2	Horizontal refresh Order (MH)	"0" = Increment , "1" = Decrement
D1	Flip horizontal (RSMX)	"0" = Normal , "1" = Horizontal flip
D0	Flip vertical (RSMY)	"0" = Normal , "1" = Vertical flip

Restriction

-

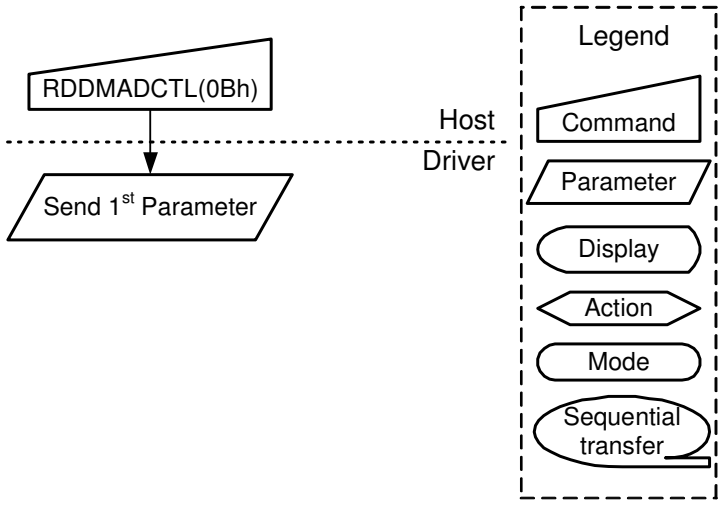
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDCOLMOD: Read Display Pixel Format (0C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDCOLMOD	Read	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Defined	Set to "0" (not used)
D6 ~ D4	RGB Interface Color Format	"101" = 16-bit / pixel "110" = 18-bit / pixel "111" = 24-bit / pixel
D3	Not Defined	Set to "0" (not used)
D2 ~ D0	Control Interface Color Format	"101" = 16-bit / pixel "110" = 18-bit / pixel "111" = 24-bit / pixel

Restriction

-

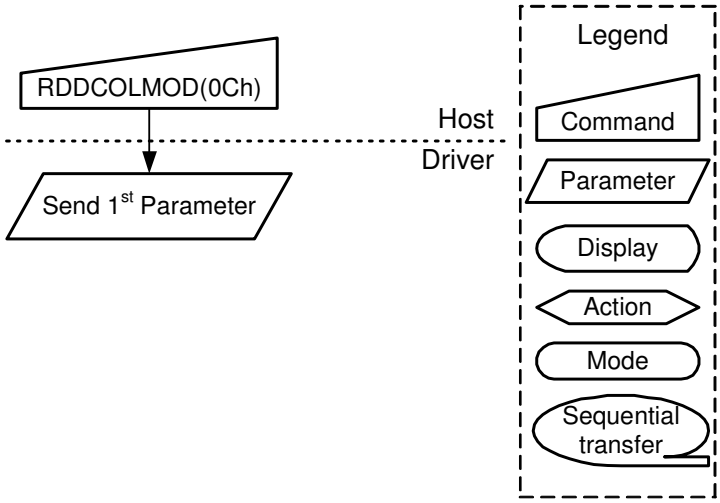
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



RDDIM: Read Display Image Mode (0D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDIM	Read	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Vertical Scrolling On/Off	Set to "0" (not used)
D6	Horizontal Scrolling On/Off	Set to "0" (not used)
D5	Inversion On/Off	"1" = Inversion On, "0" = Inversion Off
D4	All Pixel On	"1" = White display, "0" = Normal display
D3	All Pixel Off	"1" = Black display, "0" = Normal display
D2 ~ D0	Gamma Curve Selection	"000" = GC0, "001" = GC1 "010" = GC2, "011" = GC3 "100" to "111" = not defined

Restriction

-

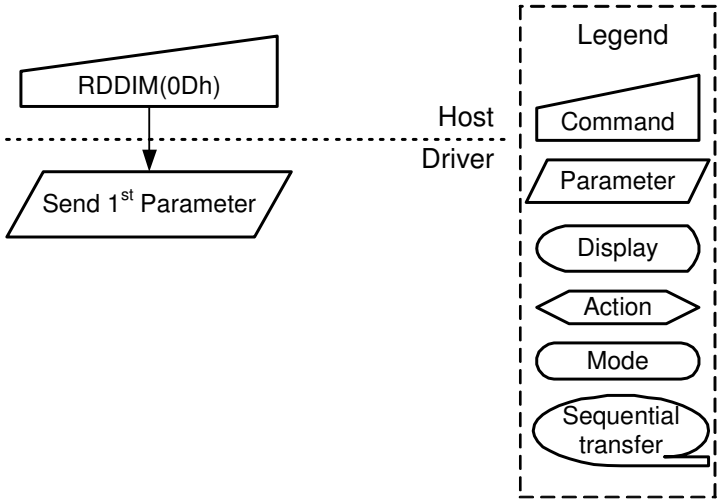
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDSM: Read Display Signal Mode (0E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDSM	Read	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing Effect Line Mode	"1" = Mode 2, "0" = Mode 1
D5	Horizontal Sync. (HS, RGB I/F)On/Off	"1" = HS bit is "1", "0" = HS bit is "0"
D4	Vertical Sync. (VS, RGB I/F)On/Off	"1" = VS bit is "1", "0" = VS bit is "0"
D3	Pixel Clock (PCLK, RGB I/F)On/Off	"1" = PCLK line is On, "0" = PCLK line is Off
D2	Data Enable (DE, RGB I/F)On/Off	"1" = DE bit is "1", "0" = DE bit is "0"
D1	Not Defined	Set to "0" (not used)
D0	Error on DSI	"1" = Error, "0" = No Error

Note: Bit D5 to D2 indicate current status of the lines when this command has been sent.

Restriction

-

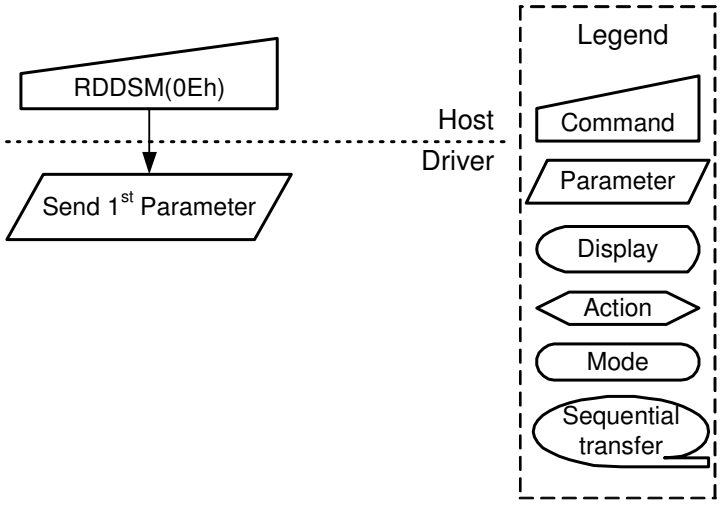
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDSDR: Read Display Self-Diagnostic Result (0F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDSDR	Read	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See section 5.13
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Defined	Set to "0" (not used)
D2	Not Defined	Set to "0" (not used)
D1	Not Defined	Set to "0" (not used)
D0	Checksums Comparison	"0": Checksums are the same "1": Checksums are not the same

Restriction

-

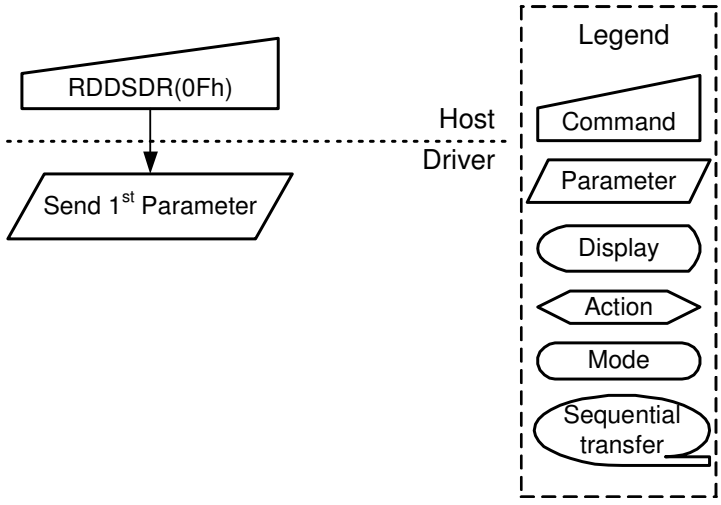
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



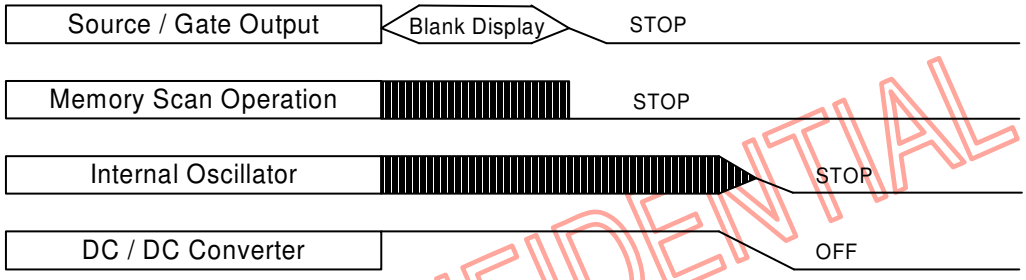
SLPIN: Sleep In (1000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPIN	Write	10h	1000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command causes the TFT LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



Control Interface as will as memory and registers are still working and the memory keeps (RAMKP="1") or loses (RAMKP="0") its contents.
User can send PCLK, HS and VS information on RGB I/F for blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode.
Dimming function does not work when there is changing mode from Sleep Out to Sleep In.
There is used an internal oscillator for blank display.

Restriction

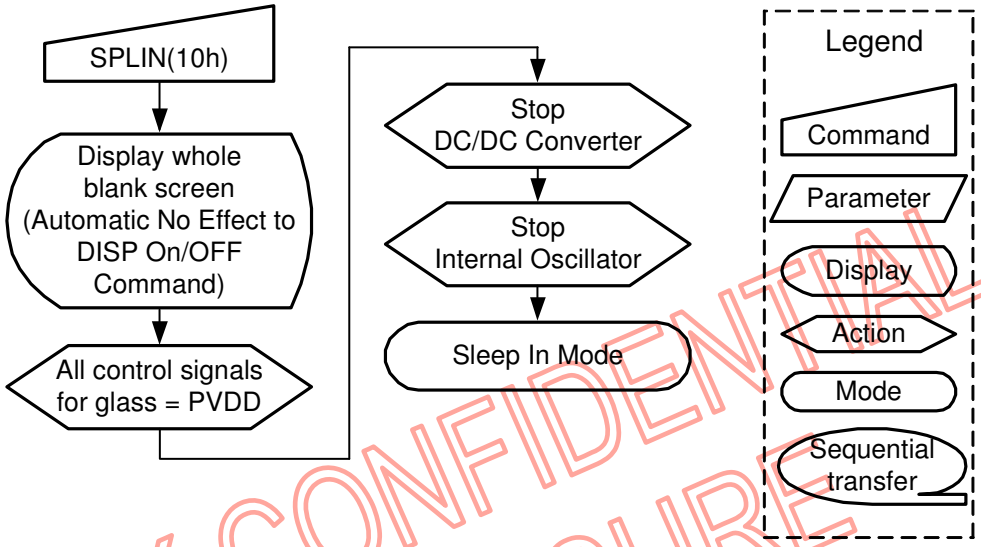
This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (0Ah) command D7. 

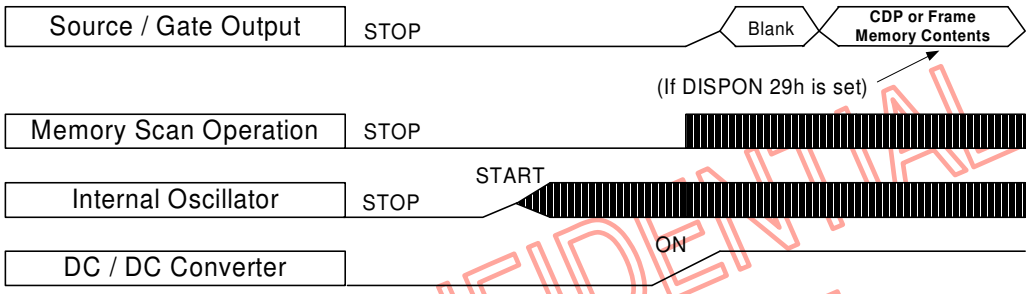
SLPOUT: Sleep Out (1100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
SLPOUT	Write	11h	1100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command turns off sleep mode.
In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.



User can start to send PCLK, HS and VS information on RGB I/F before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In-mode to Sleep Out-mode in Normal Mode On.
There is used an internal oscillator for blank display.
NT35510 will do sequence control about gate control signals when sleep out.

Restriction

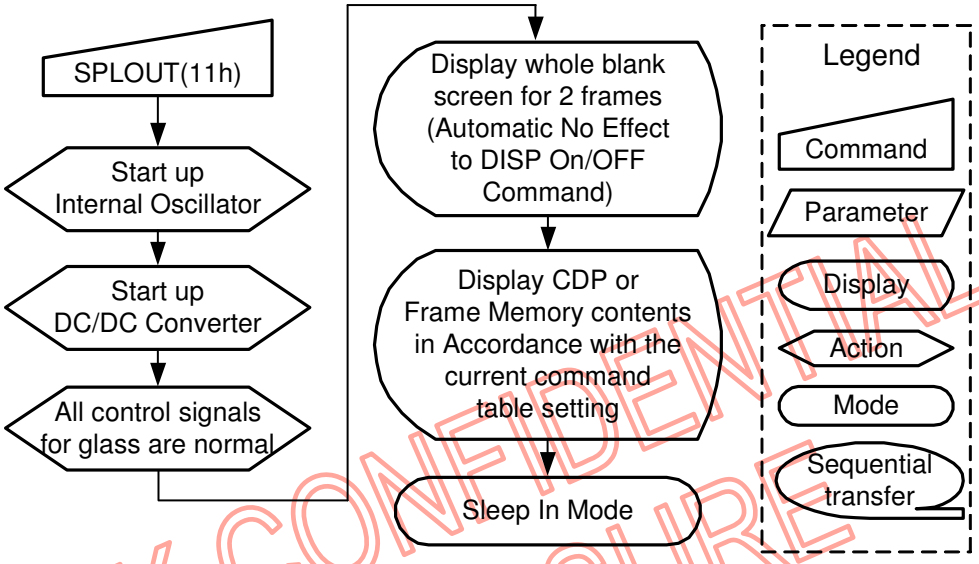
Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W reset command (01h) or H/W reset.
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
NT35510 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT35510 is already Sleep Out –mode.
NT35510 is doing self-diagnostic functions during this 5msec. See also section 5.13.
It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart	It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued. The results of booster off can be check by RDDST (0Ah) command D7. 

PTLON: Partial Display Mode On (1200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PTLON	Write	12h	1200h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command turns on Partial mode. The partial mode window is described by the Partial Area command (30H) To leave Partial mode, the Normal Display Mode On command (13H) should be written. There is no abnormal visual effect during mode change between Normal mode On to Partial mode On.
Restriction	This command has no effect when Partial Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area (30h)

NORON: Normal Display Mode On (1300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
NORON	Write	13h	1300h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) There is no abnormal visual effect during mode change from Partial mode On to Normal mode On.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart	See Partial Area Definition Descriptions for details of when to use this command

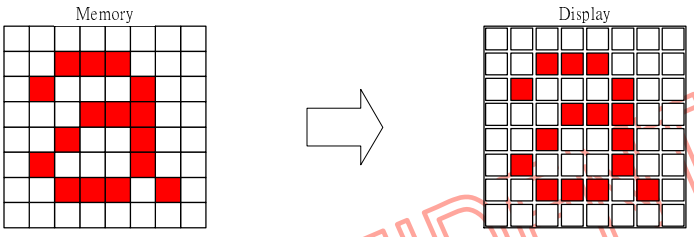
INVOFF: Display Inversion Off (2000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVOFF	Write	20h	2000h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already in Inversion Off mode.

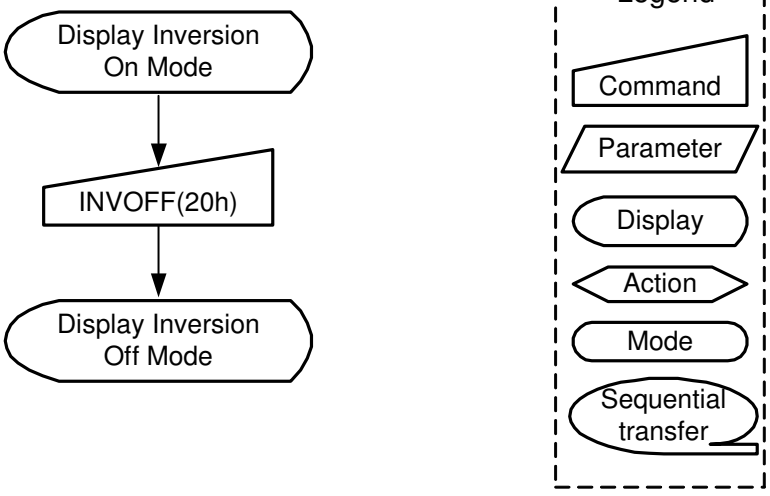
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



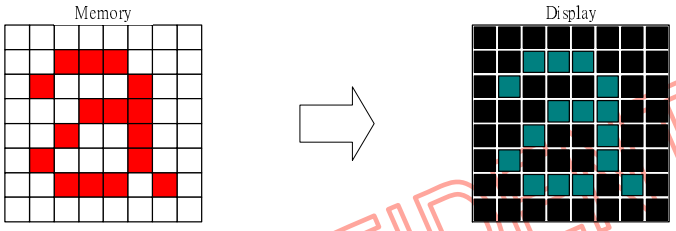
INVON: Display Inversion On (2100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
INVON	Write	21h	2100h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to enter display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.
(Example)



Restriction

This command has no effect when module is already in Inversion On mode.

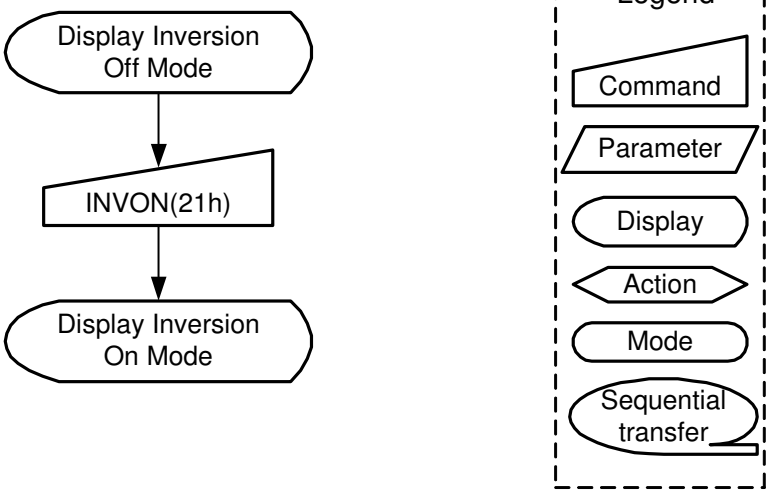
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion off
S/W Reset	Display Inversion off
H/W Reset	Display Inversion off

Flow Chart



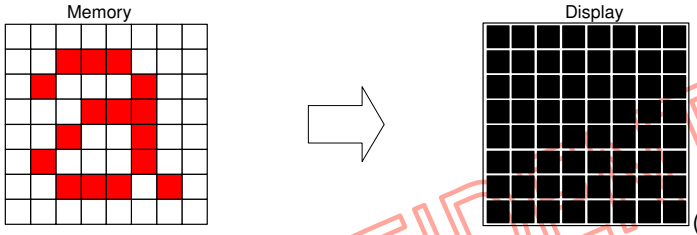
ALLPOFF: All Pixel Off (2200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPOFF	Write	22h	2200h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.
This command makes no change of contents of frame memory.
This command does not change any other status.



(Example)

"All Pixels On", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.

Restriction

This command has no effect when module is already in All Pixel Off mode.

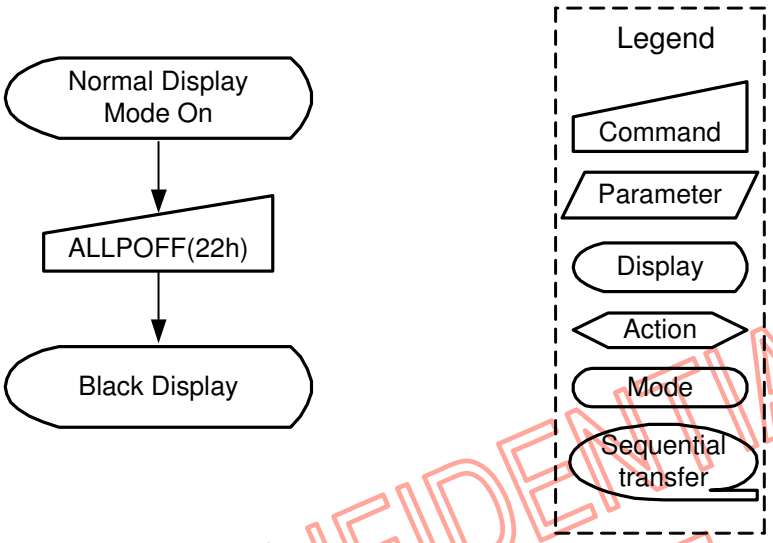
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

Flow Chart



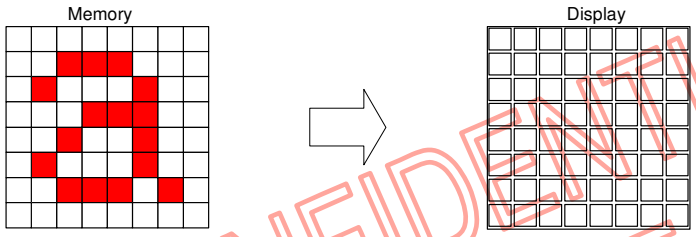
ALLPON: All Pixel On (2300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
ALLPON	Write	23h	2300h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



"All Pixels Off", "Normal Display Mode On" or "Partial Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" and "Partial Mode On" commands.

Restriction

This command has no effect when module is already in all Pixel On mode.

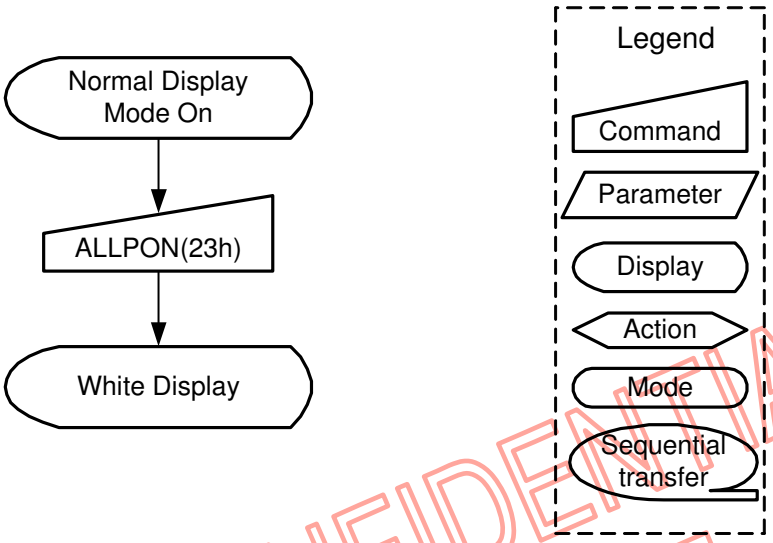
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All pixel off
S/W Reset	All pixel off
H/W Reset	All pixel off

Flow Chart



GAMSET: Gamma Set (2600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GAMSET	Write	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

NOTE: "-" Don't care

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G=2.2)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Note: All other values are undefined.

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.

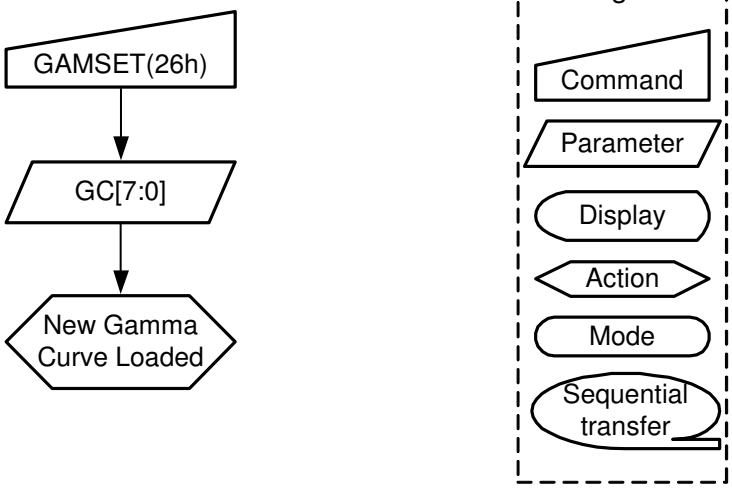
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



DISPOFF: Display Off (2800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPOFF	Write	28h	2800h	No Argument (0000h in MDDI I/F)								

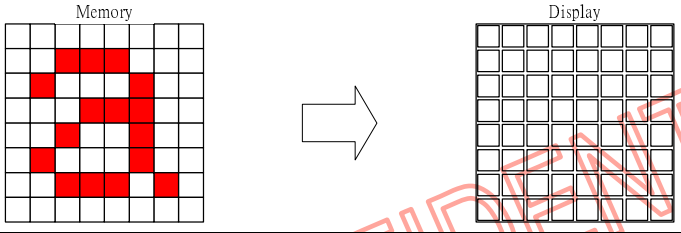
NOTE: "-" Don't care

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disables and blank page inserted.

This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

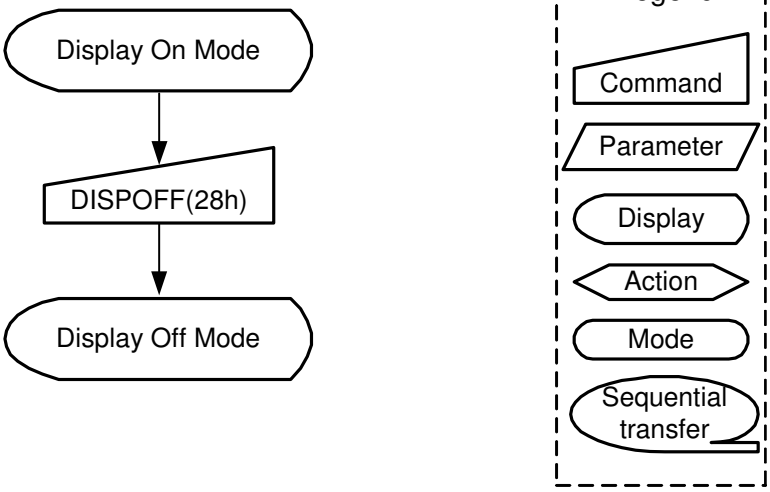
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



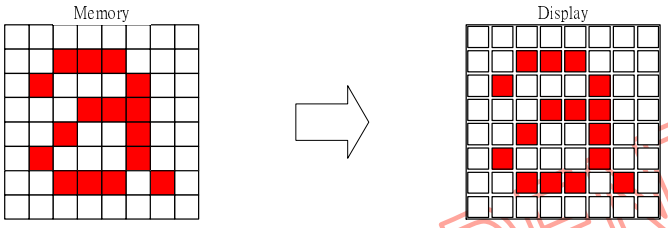
DISPON: Display On (2900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DISPON	Write	29h	2900h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to recover from DISPLAY OFF mode. Output from Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already in Display On mode.

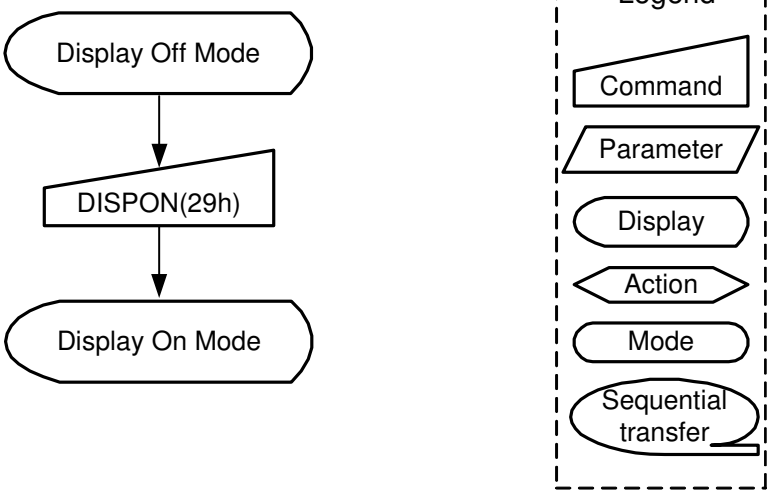
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display off
S/W Reset	Display off
H/W Reset	Display off

Flow Chart



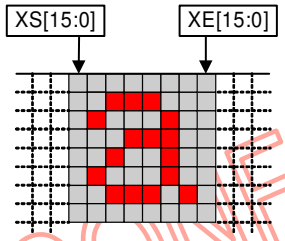
CASET: Column Address Set (2A00h~2A03h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
CASET	Write	2Ah	2A00h	00h	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8
			2A01h	00h	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0
			2A02h	00h	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8
			2A03h	00h	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0

NOTE: "-" Don't care

Description

This command is used to define area of frame memory where MPU can access.
This command makes no change on the other driver status.
Each value represents one column line in the Frame Memory.
(Example)



Restriction

XS[15:0] always must be equal to or less than XE[15:0]
When XS[15:0] or XE[15:0] is greater than maximum address like below, data of out of range will be ignored.
For CGM[7:0] = "70h" (480 x 864 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 863 (035Fh)
For CGM[7:0] = "6Bh" (480 x 854 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 853 (0355h)
For CGM[7:0] = "50h" (480 x 800 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 799 (031Fh)
For CGM[7:0] = "28h" (480 x 720 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 719 (02CFh)
For CGM[7:0] = "00h" (480 x 640 resolution)
MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 639 (027Fh)

Register Availability

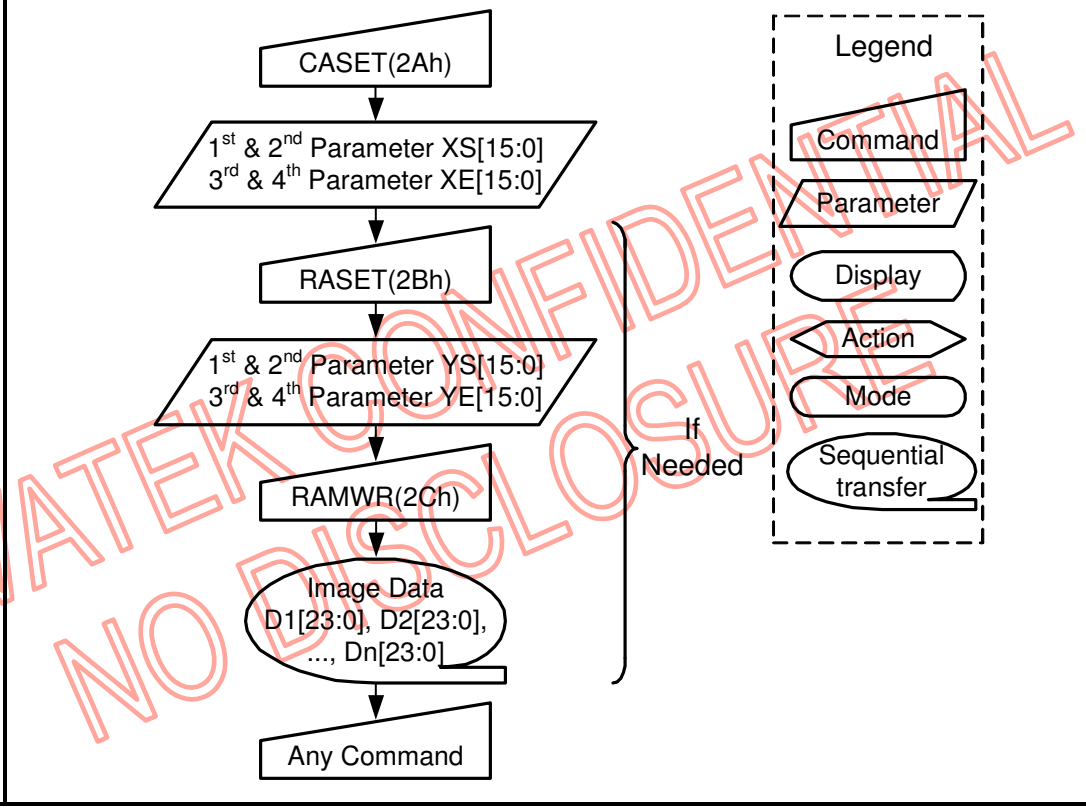
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For CGM[7:0] = “70h”, “6Bh”, “50h”, “28h”, “00h” , “FEh” (480x864/854/800/720/640 resolution)

Status	Default Value	
	XS[15:0]	XE[15:0]
Power On Sequence	0000h	01DFh (479d)
S/W Reset	0000h	01DFh (479d)
H/W Reset	0000h	01DFh (479d)

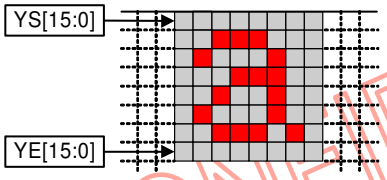
Flow Chart



RASET: Row Address Set (2B00h~2B03h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RASET	Write	2Bh	2B00h	00h	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8
			2B01h	00h	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0
			2B02h	00h	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8
			2B03h	00h	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0

NOTE: "-" Don't care

Description	This command is used to define area of frame memory where MPU can access. This command makes no change on the other driver status. Each value represents one column line in the Frame Memory. (Example) 
Restriction	YS[15:0] always must be equal to or less than YE[15:0] When YS[15:0] or YE[15:0] is greater than maximum address like below, data of out of range will be ignored. For CGM[7:0] = "70h" (480 x 864 resolution) MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 863 (035Fh) MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh) For CGM[7:0] = "6Bh" (480 x 854 resolution) MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 853 (0355h) MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh) For CGM[7:0] = "50h" (480 x 800 resolution) MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 799 (031Fh) MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh) For CGM[7:0] = "28h" (480 x 720 resolution) MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 719 (02CFh) MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh) For CGM[7:0] = "00h" (480 x 640 resolution) MV = "0": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 639 (027Fh) MV = "1": Parameter range 0 ≦ XS[15:0] ≦ XE[15:0] ≦ 479 (01DFh)
Register Availability	

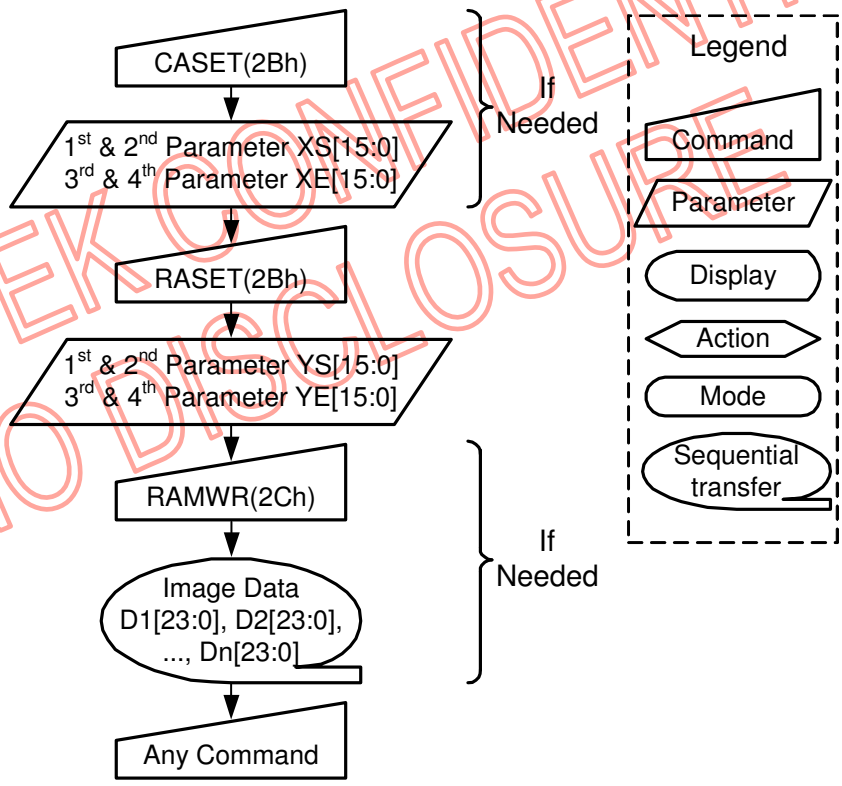
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

For CGM[7:0] = “70h”, “6Bh”, “50h”, “28h”, “00h” , “FEh” (480x864/854/800/720/640 resolution)

Status	Default Value	
	YS[15:0]	YE[15:0]
Power On Sequence	0000h	035Fh (863d)
S/W Reset	0000h	035Fh (863d) if CGM[7:0]=”70h” 0355h (853d) if CGM[7:0]=”6Bh” 031Fh (799d) if CGM[7:0]=”50h” 02CFh (719d) if CGM[7:0]=”28h” 027Fh (639d) if CGM[7:0]=”00h” 0167h (359d) if CGM[7:0]=”FEh”
H/W Reset	0000h	035Fh (863d)

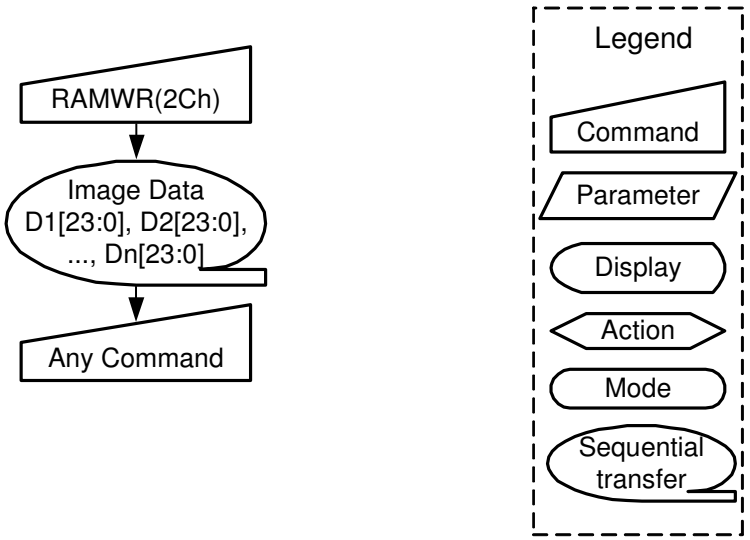
Flow Chart



RAMWR: Memory Write (2C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWR	Write	2Ch	2C00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command is used to transfer data from MPU interface to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTL setting Then D[23:0] is stored in frame memory and the column register and the row register incremented. Sending any other command can stop Frame Write.
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status: Default Value Power On Sequence: Contents of memory is set randomly S/W Reset: Contents of memory is set randomly H/W Reset: Contents of memory is set randomly
Flow Chart	

RAMRD: Memory Read (2E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRD	Read	2Eh	2E00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description	This command is used to transfer data from frame memory to MPU interface. This command makes no change to the other driver status. When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTR setting. Then D[23:0] is read back from the frame memory and the column register and the row register incremented Frame Read can be canceled by sending any other command.
Restriction	There is no restriction on length of parameters. No access in the frame memory in Sleep In mode

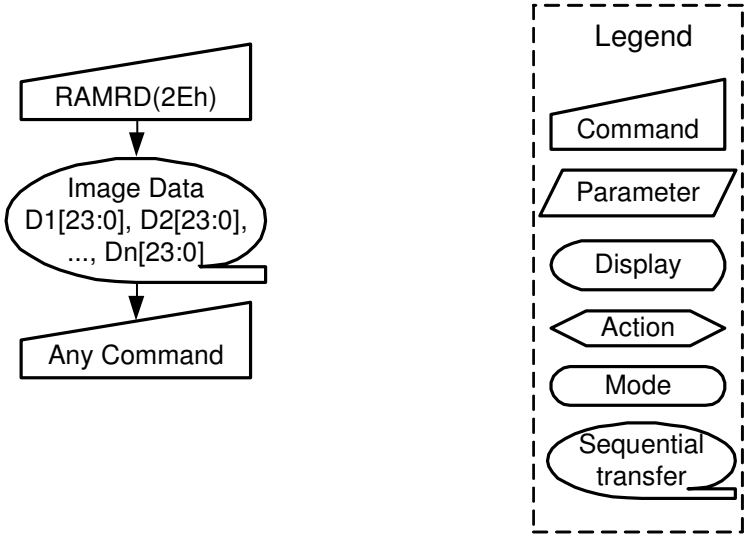
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



PTLAR: Partial Area (3000h~3003h)

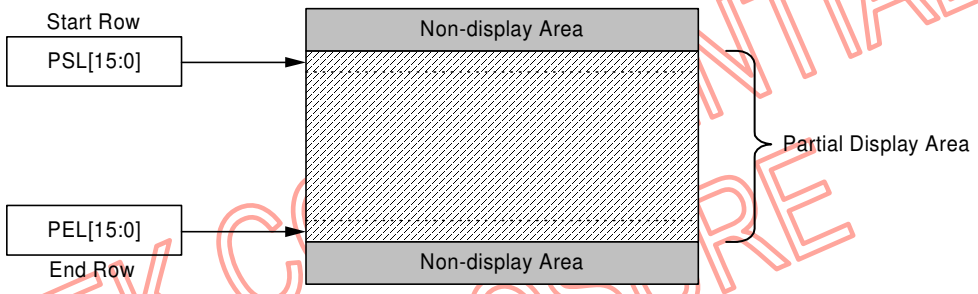
Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
PTLAR	Write	30h	3000h	00h	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8
			3001h	00h	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0
			3002h	00h	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8
			3003h	00h	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0

NOTE: "-" Don't care

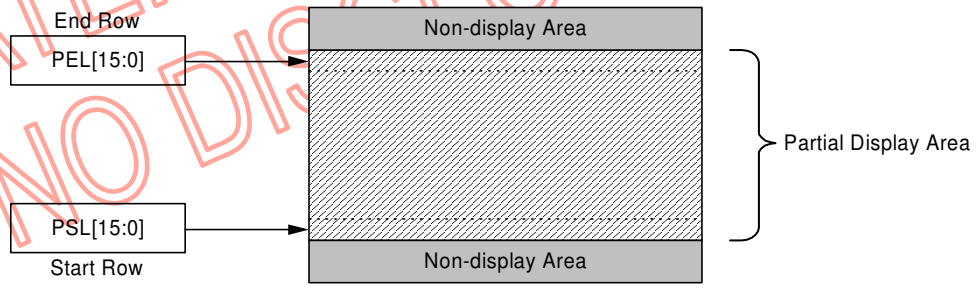
Description

This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (PSL) and the second the End Row (PEL), as illustrated in the figures below. PSL and PEL refer to the Frame Memory row address counter.

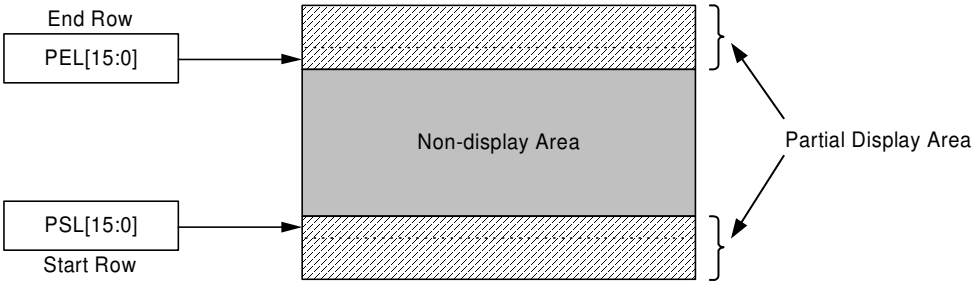
If End Row > Start Row when MADCTL ML=0:



If End Row > Start Row when MADCTL ML=1:



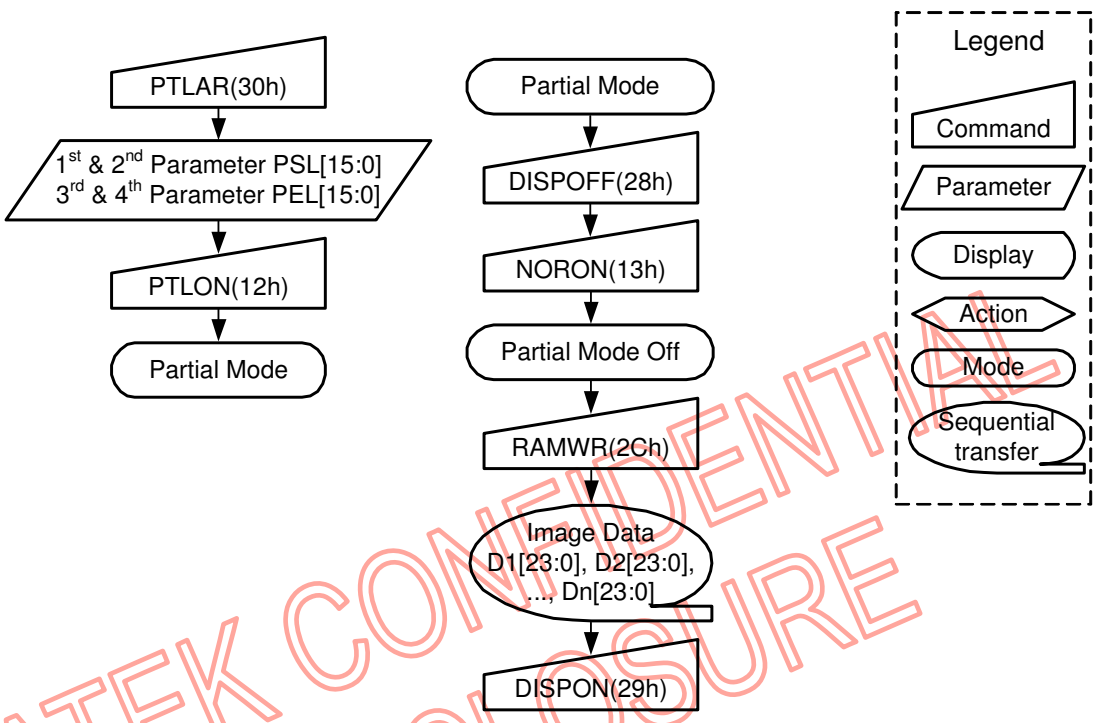
If End Row < Start Row when MADCTL ML=0:



If End Row = Start Row then the Partial Area will be one row deep.

<table>
<tr><td>Restriction</td><td>PSL[15:0] and PEL[15:0] should have below range
CGM[7:0] = ”70h” (480 x 864): 0 ≦ PSL[15:0], PEL[15:0] ≦ 863 (035Fh), |PEL–PSL| ≦ 863 (035Fh)
CGM[7:0] = ”6Bh” (480 x 854): 0 ≦ PSL[15:0], PEL[15:0] ≦ 853 (0355h), |PEL–PSL| ≦ 853 (0355h)
CGM[7:0] = ”50h” (480 x 800): 0 ≦ PSL[15:0], PEL[15:0] ≦ 799 (031Fh), |PEL–PSL| ≦ 799 (031Fh)
CGM[7:0] = ”28h” (480 x 720): 0 ≦ PSL[15:0], PEL[15:0] ≦ 719 (02CFh), |PEL–PSL| ≦ 719 (02CFh)
CGM[7:0] = ”00h” (480 x 640): 0 ≦ PSL[15:0], PEL[15:0] ≦ 639 (027Fh), |PEL–PSL| ≦ 639 (027Fh)</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>PSL[15:0]</th><th>PEL[15:0]</th></tr>
<tr><td>Power On Sequence</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
<tr><td>S/W Reset</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
<tr><td>H/W Reset</td><td>0000h</td><td>035Fh (863d) if CGM[7:0] = “70h”
0355h (853d) if CGM[7:0] = “6Bh”
031Fh (799d) if CGM[7:0] = “50h”
02CFh (719d) if CGM[7:0] = “28h”
027Fh (639d) if CGM[7:0] = “00h”
0167h (359d) if CGM[7:0] = “FEh”</td></tr>
</table>
</td></tr>
</table>

Flow Chart



TEOFF: Tearing Effect Line OFF (3400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
TEOFF	Write	34h	3400h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.

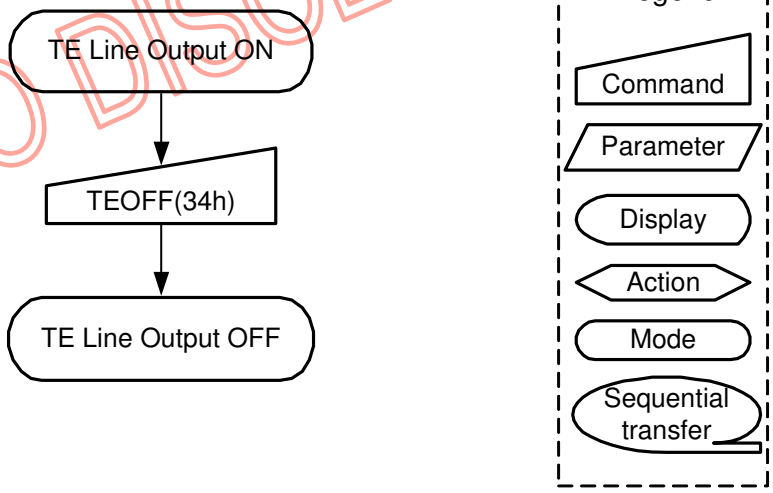
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



TEON: Tearing Effect Line ON (3500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	M

NOTE: "-" Don't care

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. ("-" = Don't Care).
When M = "0": The Tearing Effect Output line consists of V-Blanking information only.

When M = "1": The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Lofw.

Restriction

This command has no effect when Tearing Effect output is already ON.

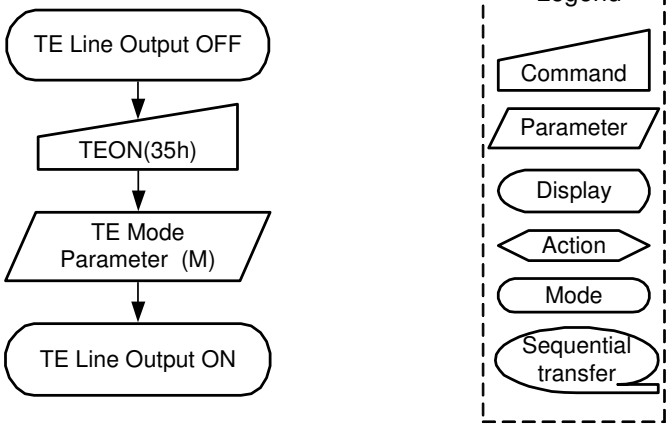
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



MADCTL: Memory Data Access Control (3600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
MADCTL	Write	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY

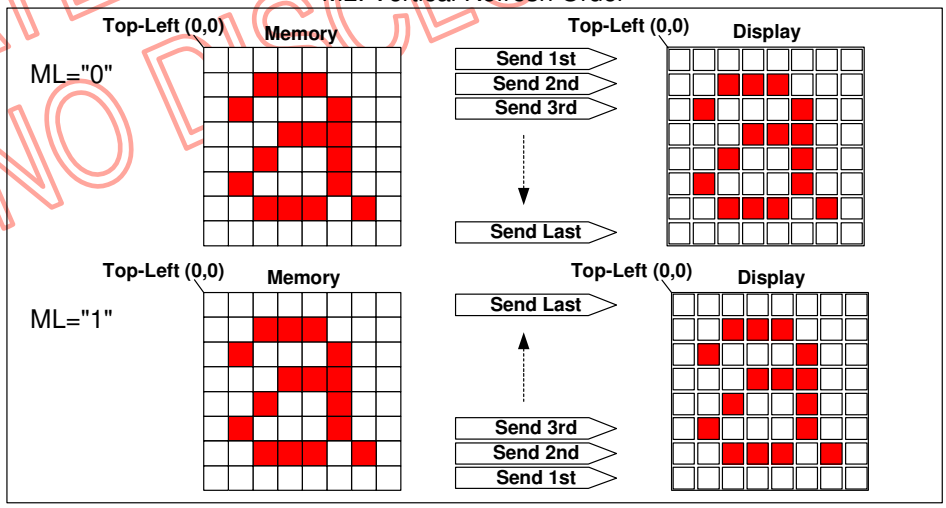
NOTE: "-" Don't care

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

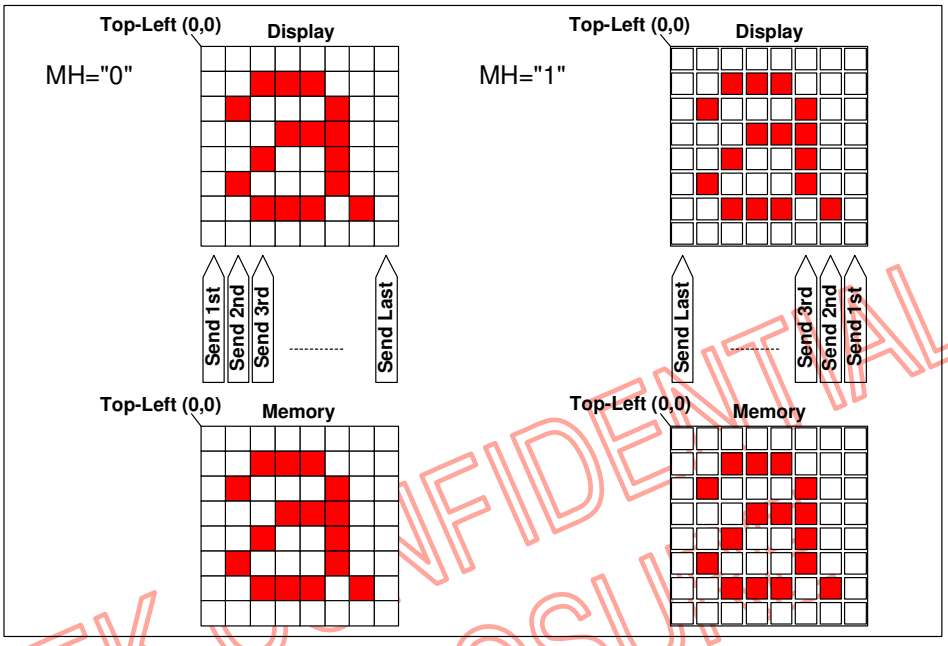
Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3 bits controls interface to memory write/read direction. The behavior on display after pattern changed.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	TFT LCD Vertical refresh direction control. Immediately behavior on display.
RGB	RGB-BGR Order	Color selector switch control "0" = RGB color sequence, "1" = BGR color sequence Immediately behavior on display
MH	Horizontal Refresh Order	TFT LCD Horizontal refresh direction control Immediately behavior on display.
RSMX	Flip Horizontal	Flips the display image left to right. Immediately behavior on display.
RSMY	Flip Vertical	Flips the display image top to down. Immediately behavior on display.

ML: Vertical Refresh Order



Description

MH: Horizontal Refresh Order



Restriction

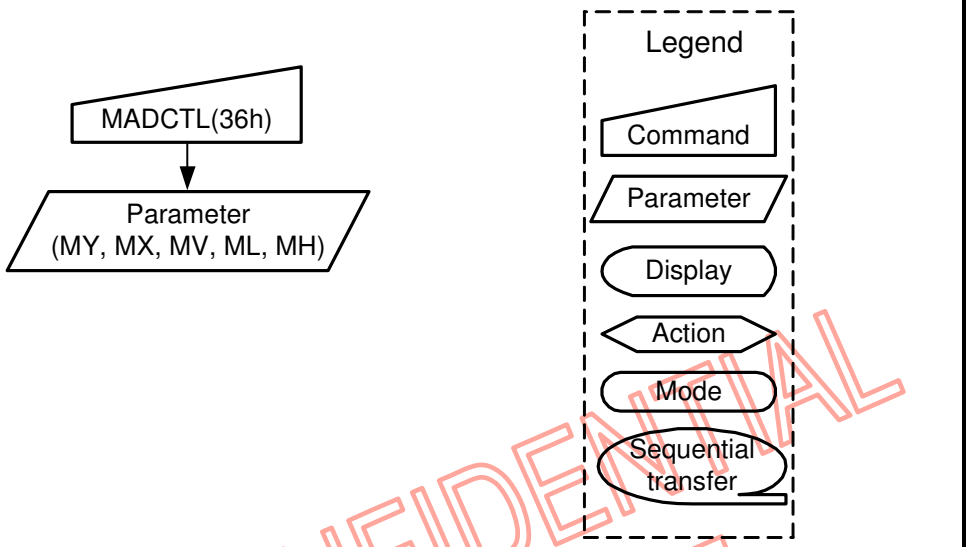
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

IDMOFF: Idle Mode Off (3800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMOFF	Write	38h	3800h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description	This command is used to recover from Idle mode on In the idle off mode, display panel can display maximum 16.7M colors.
Restriction	This command has no effect when module is already in Idle Off mode.

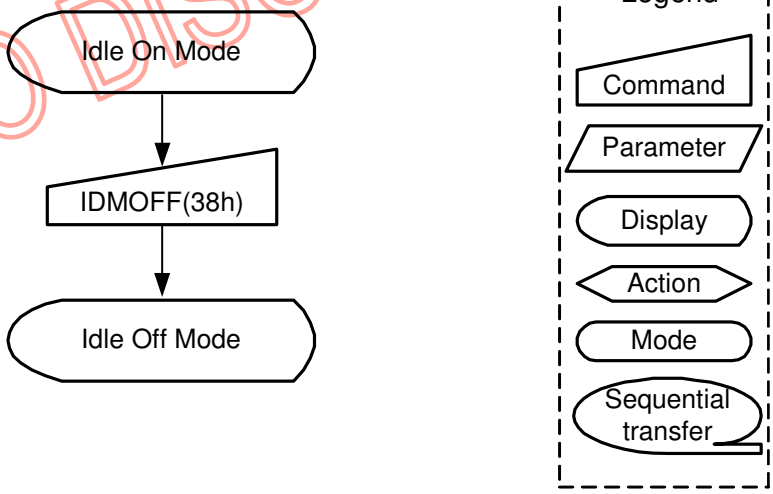
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart



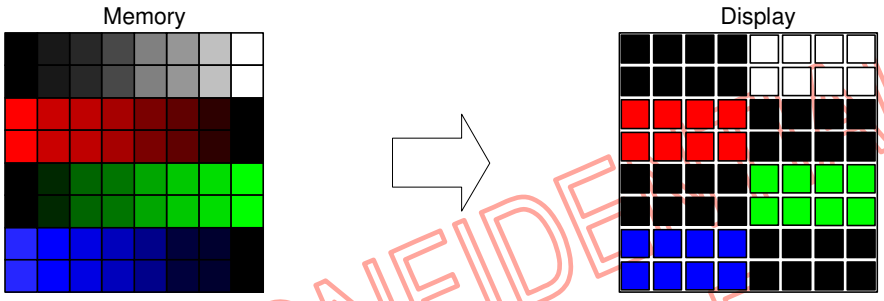
IDMON: Idle Mode On (3900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
IDMON	Write	39h	3900h	No Argument (0000h in MDDI I/F)								

NOTE: "-" Don't care

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Colors			
	$R_7R_6R_5R_4R_3R_2R_1R_0$	$R_7G_6G_5G_4G_3G_2G_1G_0$	$B_7B_6B_5B_4B_3B_2B_1B_0$
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX
Magenta	1XXXXXXX	0XXXXXXX	1XXXXXXX
Green	0XXXXXXX	1XXXXXXX	0XXXXXXX
Cyan	0XXXXXXX	1XXXXXXX	1XXXXXXX
Yellow	1XXXXXXX	1XXXXXXX	0XXXXXXX
White	1XXXXXXX	1XXXXXXX	1XXXXXXX

Restriction

This command has no effect when module is already in Idle On mode

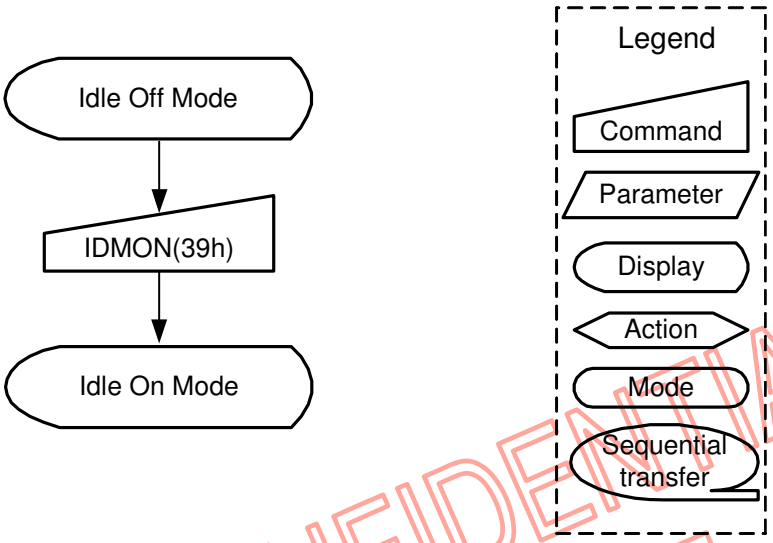
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode off
S/W Reset	Idle Mode off
H/W Reset	Idle Mode off

Flow Chart



COLMOD: Interface Pixel Format (3A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
COLMOD	Write	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0

NOTE: "-" Don't care

Description

This command is used to define the format of RGB picture data, which is to be transferred via the RGB interface. The formats are shown in the table:

Bit	NAME	DESCRIPTION
VIPF3	Pixel Format for RGB Interface	"0101" = 16-bit/pixel "0110" = 18-bit/pixel "0111" = 24-bit/pixel The others = not defined
VIPF2		
VIPF1		
VIPF0		
IFPF3	Pixel Format for Control Interface	"0101" = 16-bit/pixel "0110" = 18-bit/pixel "0111" = 24-bit/pixel The others = not defined
IFPF2		
IFPF1		
IFPF0		

Restriction

There is no visible effect until the Frame Memory is written to.

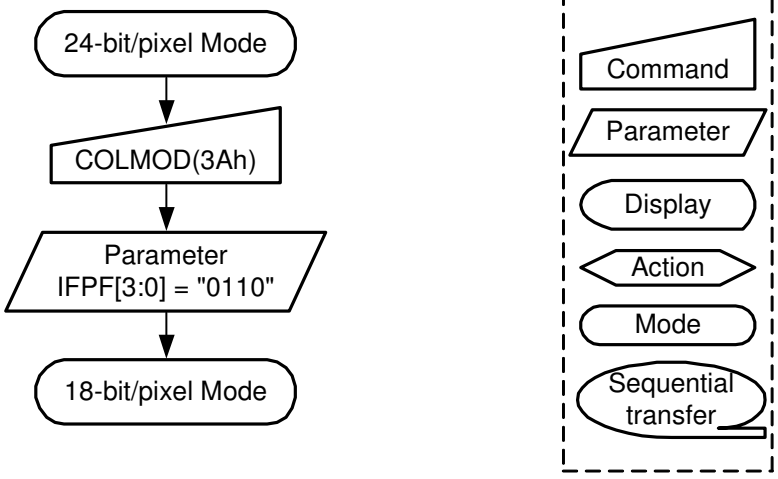
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	77h
S/W Reset	77h
H/W Reset	77h

Flow Chart



RAMWRC: Memory Write Continue (3C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMWRC	Write	3Ch	3C00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command is used to transfer data from MPU interface to frame memory, if there is wanted to continue memory write after "RAMWR Memory Write (2Ch)" command.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTL setting
Then D[23:0] is stored in frame memory and the column register and the row register incremented.
Sending any other command can stop Frame Write.

Restriction

There is no restriction on length of parameters. No access in the frame memory in Sleep In mode

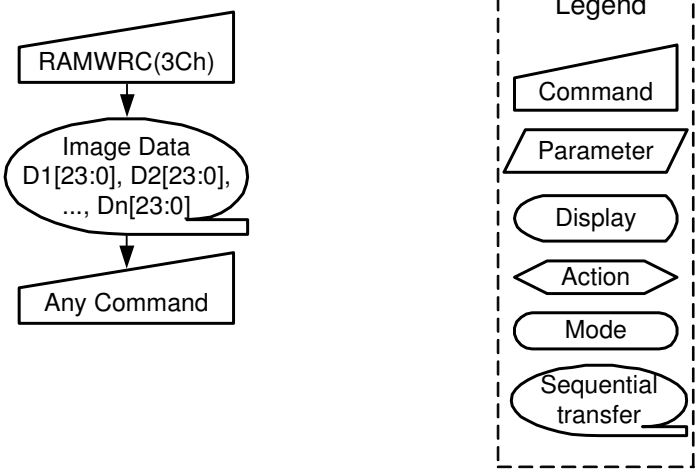
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



RAMRDC: Memory Read Continue (3E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RAMRDC	Read	3Eh	3E00h	D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0
				D[15:8]	:	:	:	:	:	:	:	:
				D[15:8]	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: "-" Don't care

Description

This command is used to transfer data from frame memory to MPU interface, if there is wanted to continue memory write after "RAMRD Memory Read (2Eh)" command.
This command makes no change to the other driver status.
When this command is accepted, the column register and the row register are not reset to the Start Column/Start Row positions.
The Start Column/Start Row positions are different in accordance with MADCTR setting.
Then D[23:0] is read back from the frame memory and the column register and the row register incremented
Frame Read can be canceled by sending any other command.

Restriction

There is no restriction on length of parameters. No access in the frame memory in Sleep In mode

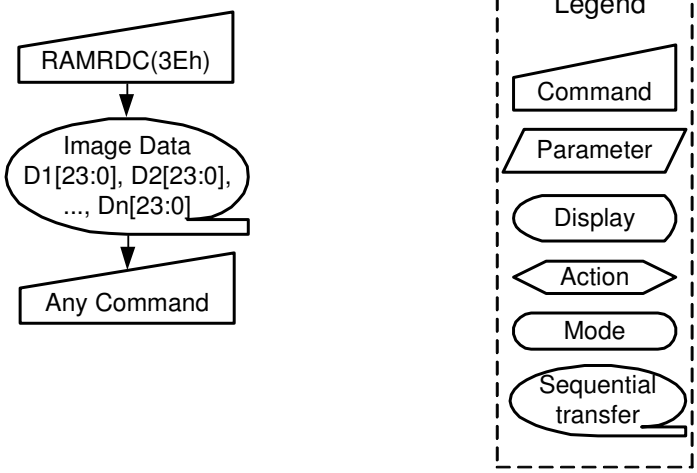
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



STESL: Set Tearing Effect Scan Line (4400h~4401h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
STESL	Write	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8
			4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0

NOTE: "-" Don't care

Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML.
The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.

Note that STESL with N[15:0]="000h" is equivalent to TEON with M="0"
The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.
This command takes affect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.

Restriction

When N[15:0] is greater than maximum scanning line like below, data of out of range will be ignored.
For CGM[7:0] = "70h" (480 x 864 resolution)
Parameter range 0 ≦ N[15:0] ≦ 864 (0360h)
For CGM[7:0] = "6Bh" (480 x 854 resolution)
Parameter range 0 ≦ N[15:0] ≦ 854 (0356h)
For CGM[7:0] = "50h" (480 x 800 resolution)
Parameter range 0 ≦ N[15:0] ≦ 800 (0320h)
For CGM[7:0] = "28h" (480 x 720 resolution)
Parameter range 0 ≦ N[15:0] ≦ 720 (02D0h)
For CGM[7:0] = "00h" (480 x 640 resolution)
Parameter range 0 ≦ N[15:0] ≦ 640 (0280h)

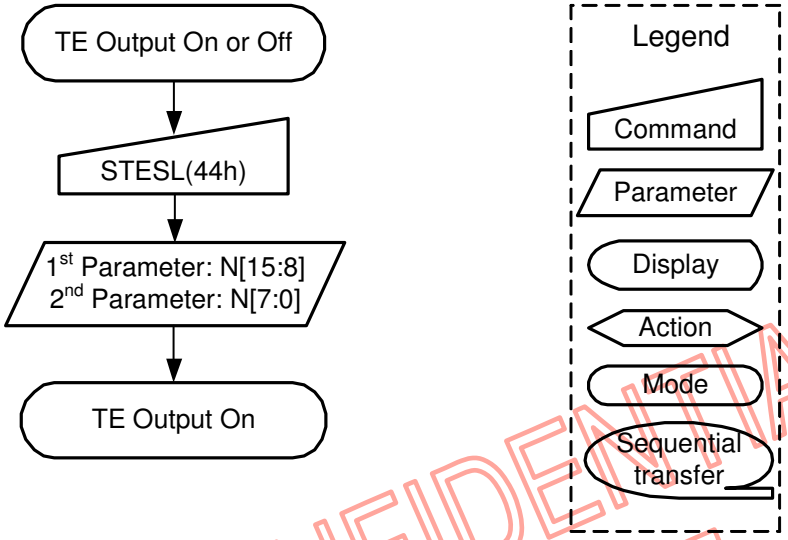
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



GSL: Get Scan Line (4500h~4501h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
GSL	Read	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8
			4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0

NOTE: "-" Don't care

Description

This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC + VBP + VADR + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0.
When in Sleep in mode, the returned value is undefined.

Restriction

-

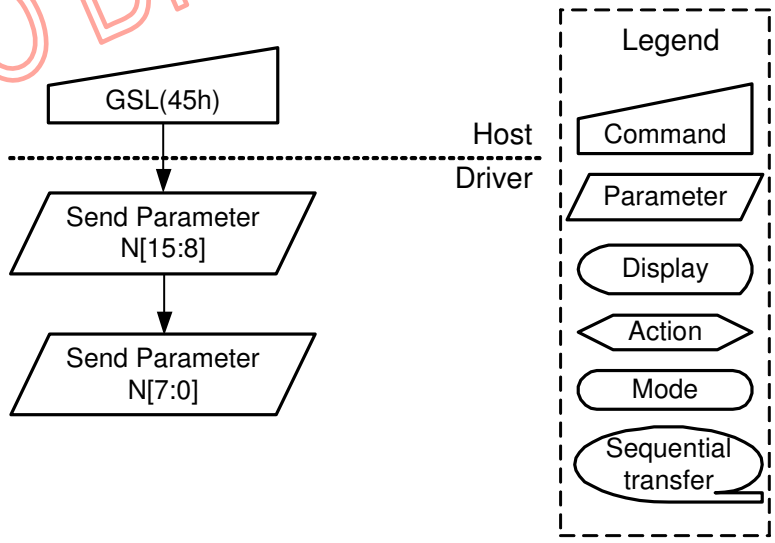
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	XXXXh
S/W Reset	XXXXh
H/W Reset	XXXXh

Flow Chart



DPCKRGB: Display Clock in RGB Interface (4A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DPCKRGB	Write	X	4A00h	00h	0	0	0	0	0	0	0	ICM

NOTE: "-" Don't care

Description

This command is used to select SRAM data input path and display clock in RGB interface.

ICM	Data Write to SRAM		SRAM Data Read to Display
	SRAM Write Clock	SRAM Data Input Path	Internal Display Clock
0	PCLK	D[23:0]	VS, HS and PCLK
1	SCL	SDI	Internal Oscillator

Restriction

-

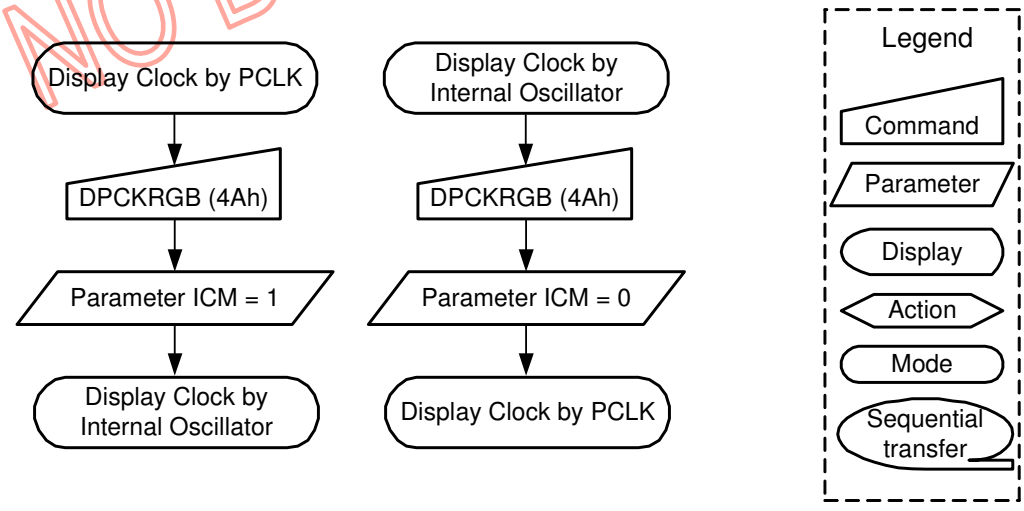
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ICM = "0"
S/W Reset	ICM = "0"
H/W Reset	ICM = "0"

Flow Chart



DSTBON: Deep Standby Mode On (4F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DSTBON	Write	X	4F00h	00h	0	0	0	0	0	0	0	DSTB

NOTE: "-" Don't care

Description

This command is used to enter deep standby mode.
DSTB="1", enter deep standby mode.
Notes:
1. Before setting this command, enter Sleep In Mode (1000h) and Display Off (2800h) first.
   User can not write this register in Sleep-Out and Display-On mode.
2. It can not exit Deep Standby Mode while setting bit DSTB from "1" to "0".
3. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.

Restriction

-

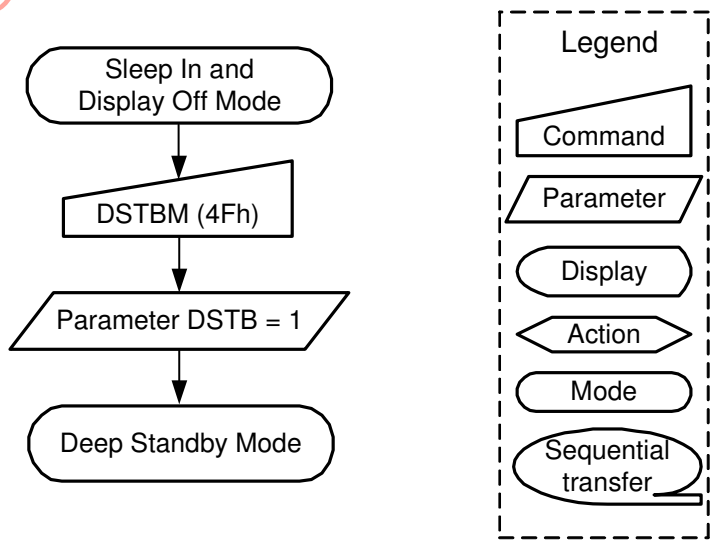
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DSTB = "0"
S/W Reset	DSTB = "0"
H/W Reset	DSTB = "0"

Flow Chart



WRPFD: Write Profile Value for Display (5000h~500Fh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRPFD	Write	50h	5000h	00h	V017	V016	V015	V014	V013	V012	V011	V010
			5001h	00h	V027	V026	V025	V024	V023	V022	V021	V020
			5002h	00h	V037	V036	V035	V034	V033	V032	V031	V030
			:	00h	:	:	:	:	:	:	:	:
			500Dh	00h	V147	V146	V145	V144	V143	V142	V141	V140
			500Eh	00h	V157	V156	V155	V154	V153	V152	V151	V150
			500Fh	00h	V167	V166	V165	V164	V163	V162	V161	V160

NOTE: "-" Don't care

Description	This command is used to define profile values for display.
Restriction	-

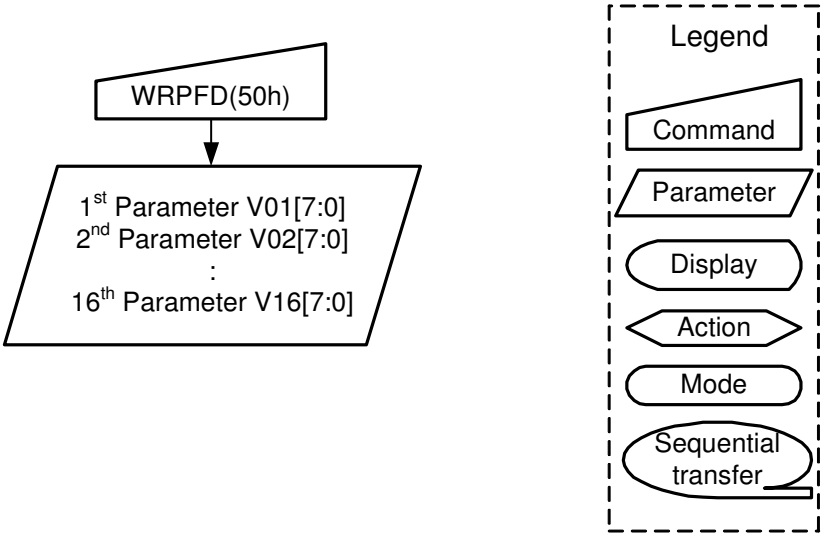
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



WRDISBV: Write Display Brightness (5100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	Write	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

NOTE: "-" Don't care

Description

This command is used to adjust brightness value.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

DBV[7:0]	Brightness (Ratio)	Brightness (%)
00h	0/256	0%
01h	2/256	0.78125%
:	:	:
FEh	255/256	99.609375%
FFh	256/256	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

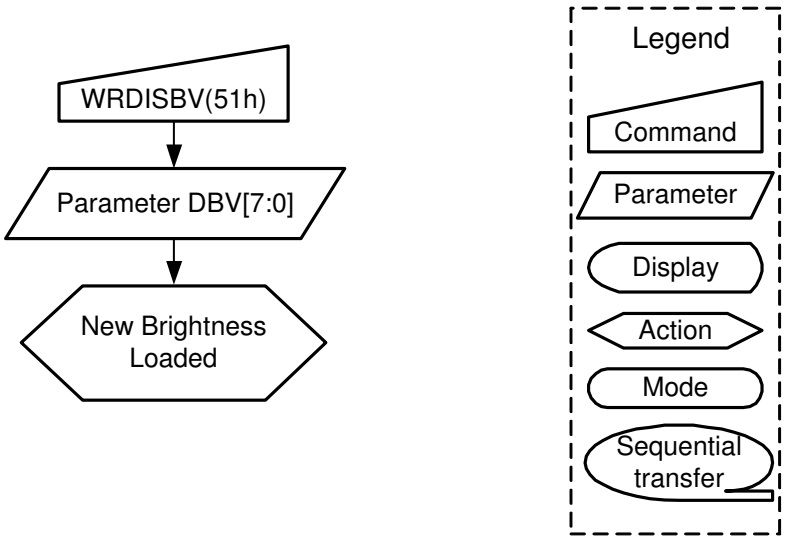
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDDISBV: Read Display Brightness (5200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDISBV	Read	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

NOTE: "-" Don't care

Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.
Restriction	-

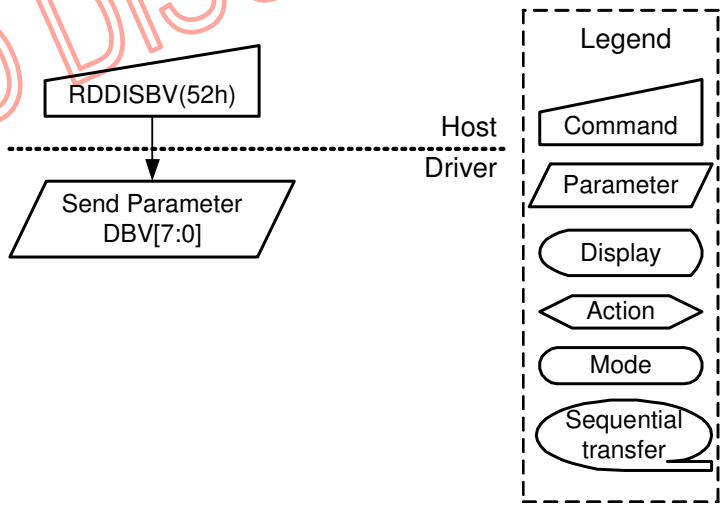
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCTRLD: Write CTRL Display (5300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	Write	53h	5300h	00h	0	0	BCTRL	A	DD	BL	DB	G

NOTE: "-" Don't care

Description

This command is used to control ambient light, brightness and gamma setting.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

A	DESCRIPTION	PWM duty for LEDPWM Pin
0	Off	By DBV[7:0] of command "WRDISBV (5100h)"
1	On	By LABC block

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": output low (for high active) LEDONPOL="1": output high (for low active)
1	On	LEDONPOL="0": output high (for high active) LEDONPOL="1": output low (for low active)

DB: Display Brightness Manual/Automatic

DB	DESCRIPTION
0	Manual, the user has to use this setting for manual adjustment of the brightness to have an effect.
1	Automatic, information about the used brightness is included in the active profile.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

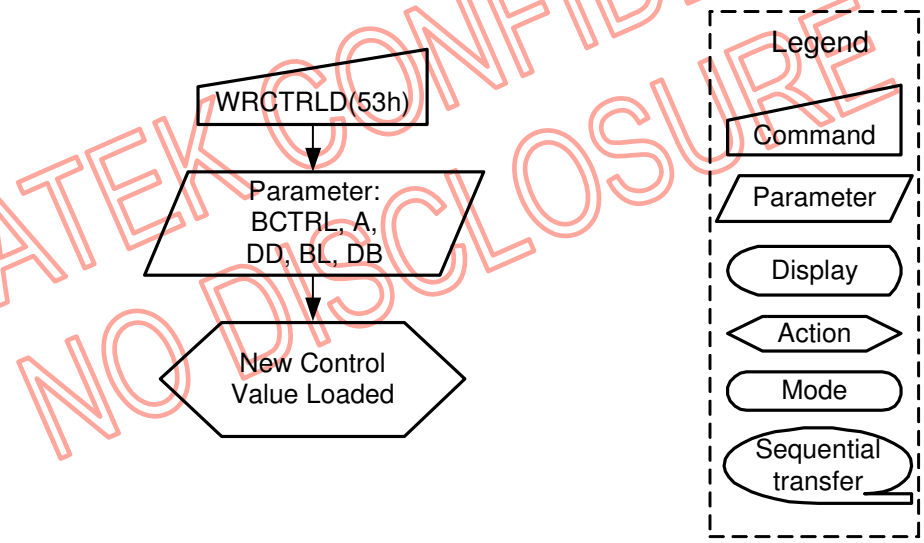
G: Gamma Curve Manual/Automatic

G	DESCRIPTION
0	Manual, by GAMSET-command
1	Automatic, information about the used gamma is included in the active profile.

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

<table>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

RDCTRLD: Read CTRL Display Value (5400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCTRLD	Read	54h	5400h	00h	0	0	BCTRL	A	DD	BL	DB	G

NOTE: "-" Don't care

Description

This command returns ambient light, brightness control and gamma setting value.

BCTRL: Brightness Control Block On/Off

The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL	DESCRIPTION	LEDPWM Pin
0	Off, DBV[7:0] and KBV[7:0] are 00h.	LEDPWPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On, DBV[7:0] and KBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

A: LABC Block On/Off

The BCTRL bit is used to control LABC block.

A	DESCRIPTION	PWM duty for LEDPWM Pin
0	Off	By DBV[7:0] of command "WRDISBV (5100h)"
1	On	By LABC block

DD: Display Dimming Control On/Off

DD	DESCRIPTION
0	Display dimming is off
1	Display dimming is on

BL: Backlight Control On/Off without Dimming Effect

When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected.

BL	DESCRIPTION	LEDON Pin
0	Off	LEDONPOL="0": PWM keep low (for high active) LEDPWPOL="1": PWM keep high (for low active)
1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)

DB: Display Brightness Manual/Automatic

DB	DESCRIPTION
0	Manual, the user has to use this setting for manual adjustment of the brightness to have an effect.
1	Automatic, information about the used brightness is included in the active profile.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

G: Gamma Curve Manual/Automatic

G	DESCRIPTION
0	Manual, by GAMSET-command
1	Automatic, information about the used gamma is included in the active profile.

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0→1 or 1→0.

When the ambient light sensing off-mode (A="0"), display brightness and gamma setting should be manual setting (DB="0" and G="0"). Setting values are the last one written with "Write Display Brightness (5100h)" command and GAMSET-command or the default one.

When the ambient light control on, light sensor control block is always working, even if backlight off (BL="0") and display brightness manual (DB="0") are selected.

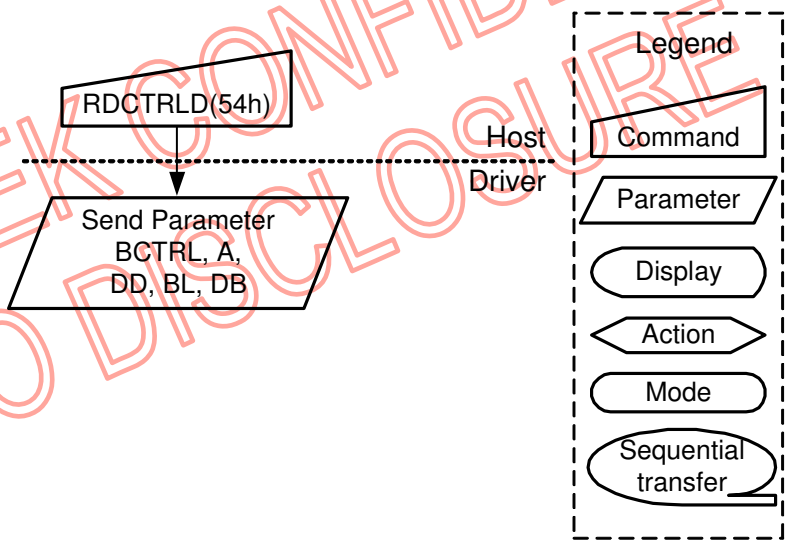
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCABC: Write Content Adaptive Brightness Control (5500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABC	Write	55h	5500h	00h	0	0	0	0	0	0	C1	C0

NOTE: "-" Don't care

Description

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Picture Image (Moving-Mode)

Restriction

This register is synchronized with V-sync by internal circuit.

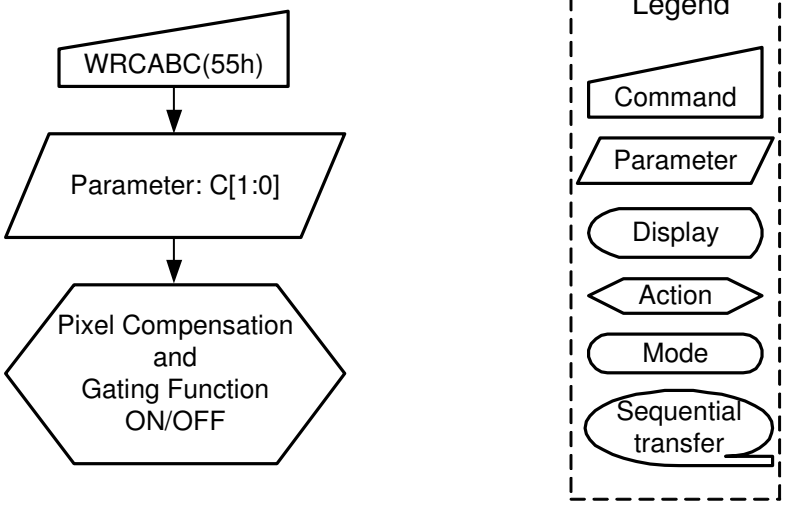
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCABC: Read Content Adaptive Brightness Control (5600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABC	Read	56h	5600h	00h	0	0	0	0	0	0	C1	C0

NOTE: "-" Don't care

Description

This command is used to read the settings for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function
0	0	Off
0	1	User Interface Image (UI-Mode)
1	0	Still Picture Image (Still-Mode)
1	1	Moving Picture Image (Moving-Mode)

Restriction

-

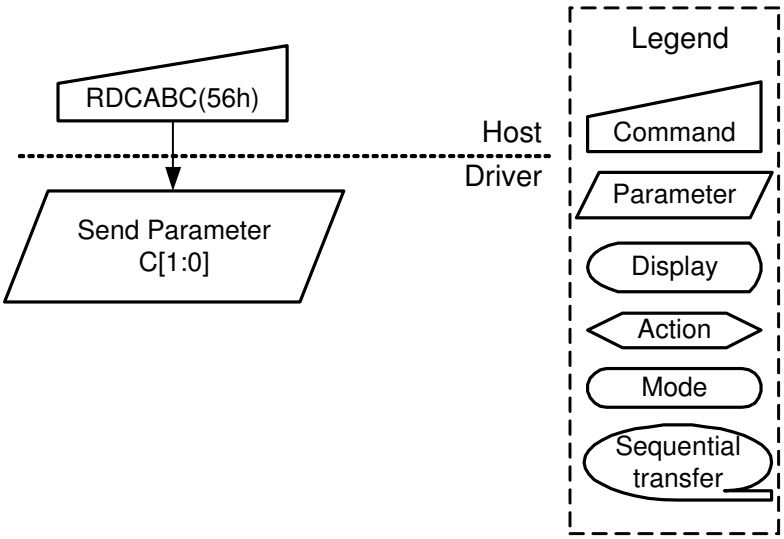
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRHYSTE: Write Hysteresis (5700h~573Fh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRHYSTE	Write	57h	5700h	00h	I0115	I0114	I0113	I0112	I0111	I0110	I019	I018
			5701h	00h	I017	I016	I015	I014	I013	I012	I011	I010
			5702h	00h	I0215	I0214	I0213	I0212	I0211	I0210	I029	I028
			5703h	00h	I027	I026	I025	I024	I023	I022	I021	I020
			:	00h	In15	In14	In13	In12	In11	In10	In9	In8
			:	00h	In7	In6	In5	In4	In3	In2	In1	In0
			571Ch	00h	I1515	I1514	I1513	I1512	I1511	I1510	I159	I158
			571Dh	00h	I157	I156	I155	I154	I153	I152	I151	I150
			571Eh	00h	I1615	I1614	I1613	I1612	I1611	I1610	I169	I168
			571Fh	00h	I167	I166	I165	I164	I163	I162	I161	I160
			5720h	00h	D0115	D0114	D0113	D0112	D0111	D0110	D019	D018
			5721h	00h	D017	D016	D015	D014	D013	D012	D011	D010
			5722h	00h	D0215	D0214	D0213	D0212	D0211	D0210	D029	D028
			5723h	00h	D027	D026	D025	D024	D023	D022	D021	D020
			:	00h	Dn15	Dn14	Dn13	Dn12	Dn11	Dn10	Dn9	Dn8
			:	00h	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0
			573Ch	00h	D1515	D1514	D1513	D1512	D1511	D1510	D159	D158
			573Dh	00h	D157	D156	D155	D154	D153	D152	D151	D010
			573Eh	00h	D1615	D1614	D1613	D1612	D1611	D1610	D169	D168
			573Fh	00h	D167	D166	D165	D164	D163	D162	D161	D160

NOTE: "-" Don't care

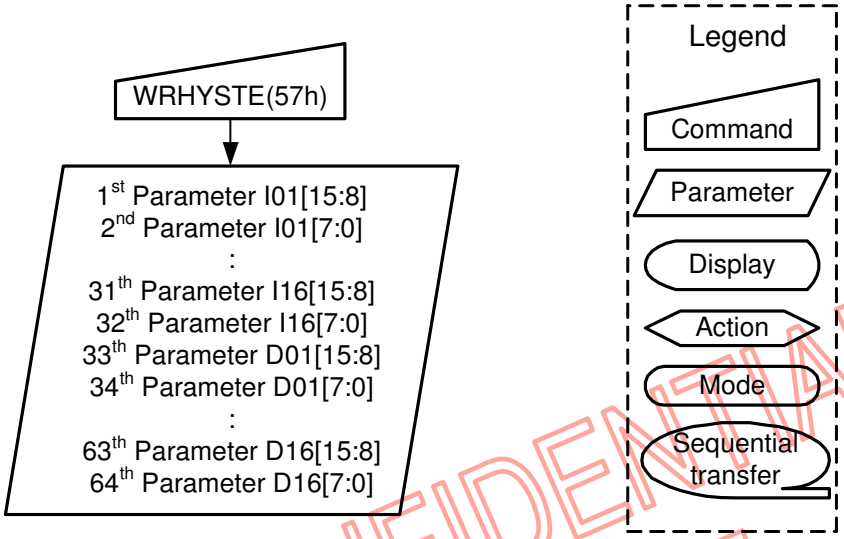
Description	This command is used to define Hysteresis filter function. In[15:0] defines increment values and Dn[15:0] defines decrement values. Don't care about the parameter values after "65535 (FFFFh)". I16[15 : 0] bits and D16[15 : 0] bits are always set to "65535 (FFFFh)" internally, if I15[15 : 0] bits and D15[15 : 0] bit are still valid and less than "65535 (FFFFh)".
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



WRGAMMSET: Write Gamma Setting (5800h~5807h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRGAMMSET	Write	58h	5800h	00h	G023	G022	G021	G020	G013	G012	G011	G010
			5801h	00h	G043	G042	G041	G040	G033	G032	G031	G030
			5802h	00h	G063	G062	G061	G060	G053	G052	G051	G050
			5803h	00h	G083	G082	G081	G080	G073	G072	G071	G070
			5804h	00h	G103	G102	G101	G100	G093	G092	G091	G090
			5805h	00h	G123	G122	G121	G120	G113	G112	G111	G110
			5806h	00h	G143	G142	G141	G140	G133	G132	G131	G130
			5807h	00h	G163	G162	G161	G160	G153	G152	G151	G150

NOTE: "-" Don't care

Description

This command is used to define gamma setting values for each luminance level.
Gamma value is defined on command "Gamma Set (2600h)".

Gn[3:0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1 (G=2.2)
02h	GC1	Reserved
04h	GC2	Reserved
08h	GC3	Reserved

Restriction

-

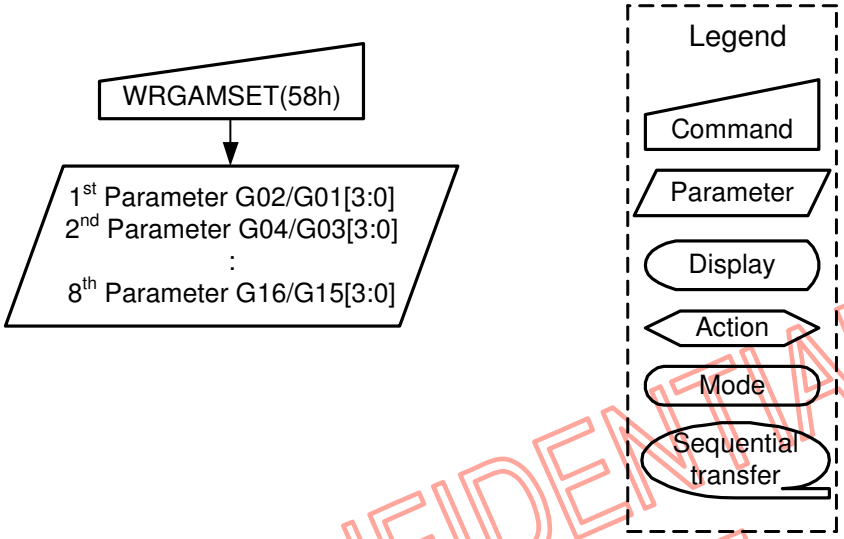
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

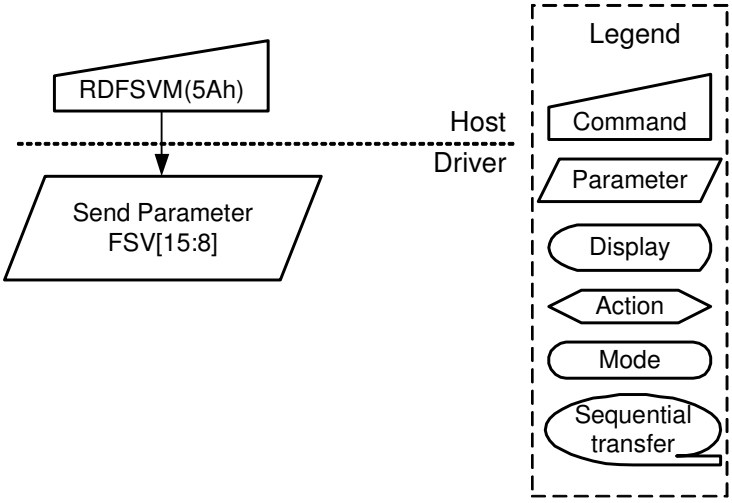
Flow Chart



RDFSVM: Read FS Value MSBs (5A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFSVM	Read	5Ah	5A00h	00h	FSV15	FSV14	FSV13	FSV12	FSV11	FSV10	FSV9	FSV8

NOTE: "-" Don't care

Description	This command returns MSBs (FSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading. Another command for LSBs (FSV[7:0]). See the command "Read FS Value LSBs (5B00h)". When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs. If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released. FSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0". *Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".*
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes
Default	Status / Default Value Power On Sequence: 00h S/W Reset: 00h H/W Reset: 00h
Flow Chart	

RDFSVL: Read FS Value LSBs (5B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFSVL	Read	5Bh	5B00h	00h	FSV7	FSV6	FSV5	FSV4	FSV3	FSV2	FSV1	FSV0

NOTE: "-" Don't care

Description

This command returns LSBs (FSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the flicker has been removed from ambient light reading.
Another command for MSBs (FSV[15:8]). See the command "Read FS Value MSBs (5A00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

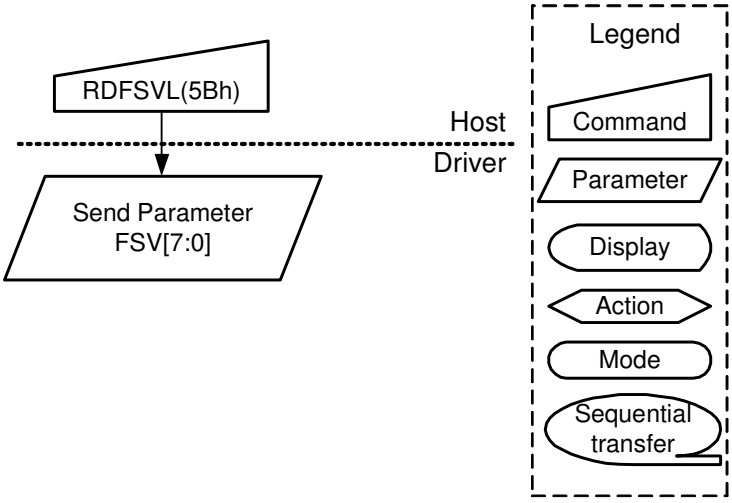
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDMFFSVM: Read Median Filter FS Value MSBs (5C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDMFFSVM	Read	5Ch	5C00h	00h	FFSV15	FFSV14	FFSV13	FFSV12	FFSV11	FFSV10	FFSV9	FFSV8

NOTE: "-" Don't care

Description

This command returns MSBs (FFSV[15:8]) of the "Front Side Ambient Light Sensor Value" after the median filter.
Another command for LSBs (FFSV[7:0]). See the command "Read Median Filter FS Value LSBs (5D00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FFSV[15:8] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FFSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

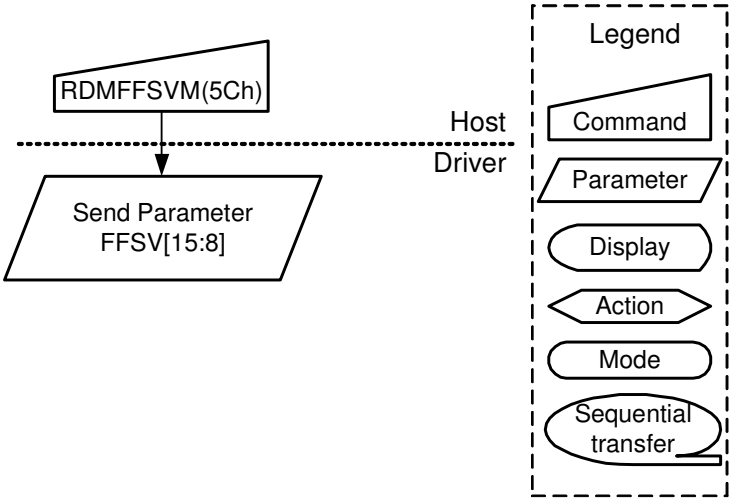
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDMFFSVL: Read Median Filter FS Value LSBs (5D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDMFFSVL	Read	5Dh	5D00h	00h	FFSV7	FFSV6	FFSV5	FFSV4	FFSV3	FFSV2	FFSV1	FFSV0

NOTE: "-" Don't care

Description

This command returns LSBs (FDSV[7:0]) of the "Front Side Ambient Light Sensor Value" after the median filter.
Another command for MSBs (FFSV[15:8]). See the command "Read Median Filter FS Value MSBs (5C00h)".
When using read LSBs/MSBs command, corresponding MSBs/LSBs should be locked so that they refer to the same value when LSBs/MSBs are read. After reading both values, registers for MSBs and LSBs should be released. And that if e.g. LSBs are read and there is no MSBs read command, the next LSBs read will also update MSBs. If MSBs are read at first, the next MSBs read will update LSBs.
If any other commands are received between LSBs read command and MSBs read command, the registers for MSBs and LSBs should be released.
FFSV[7:0] should be 00h when bit 'A' of the "Write CTRL Display (5300h)" command is "0".
Note: Although FSV[15:0] is 16-bit length register, the valid value range is 0 ~ 65535 (0000h ~ FFFFh), In other words, user don't care about the parameter values over than "65535 (FFFFh)".

Restriction

-

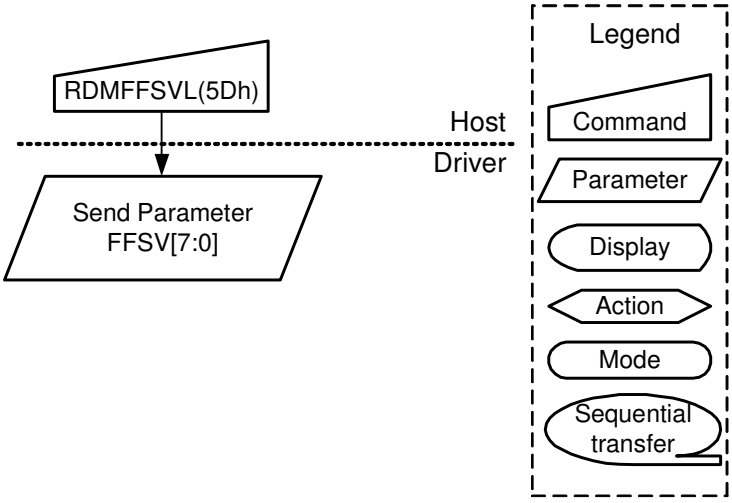
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRCABCMB: Write CABC minimum brightness (5E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCABCMB	Write	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

NOTE: "-" Don't care

Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
Restriction	-

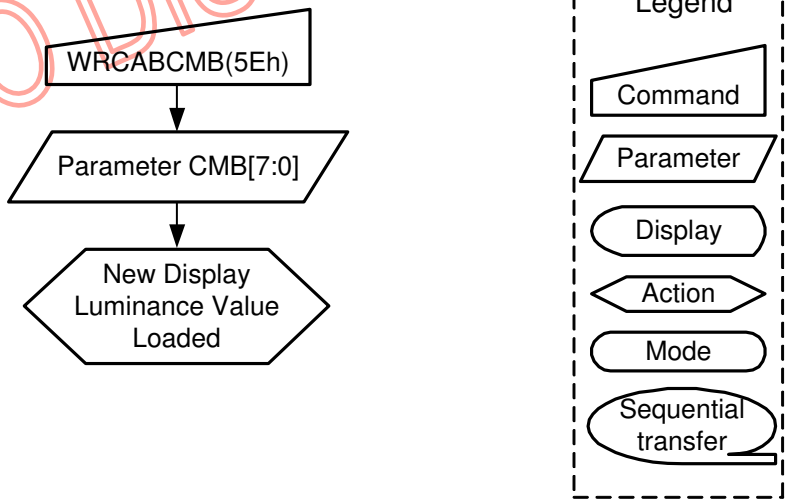
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCABCMB: Read CABC minimum brightness (5F00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCABCMB	Read	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

NOTE: "-" Don't care

Description

This command return the minimum brightness value of CABC function
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.
CMB[7:0] is minimum brightness forCABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.

Restriction

-

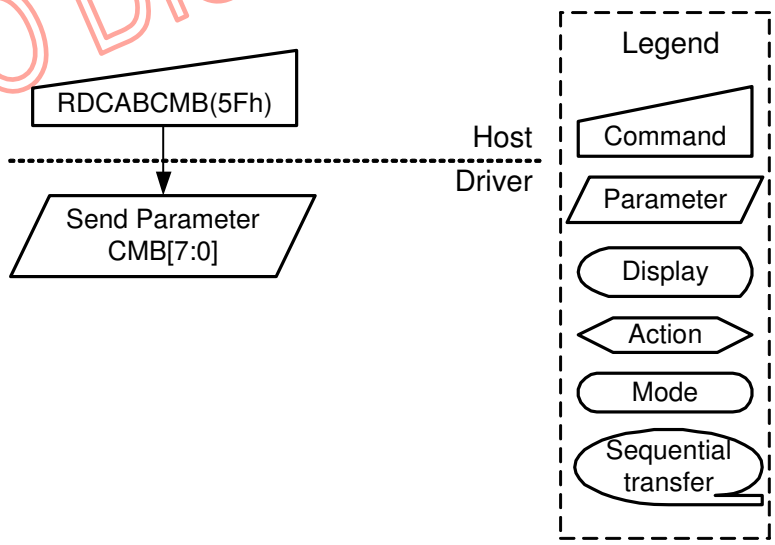
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



WRLSCC: Write Light Sensor Compensation Coefficient Value (6500h~6501h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRLSCC	Write	65h	6500h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8
			6501h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

NOTE: "-" Don't care

Description	This command is used to send the compensation coefficient value (CC[15 : 0]). Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary).
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

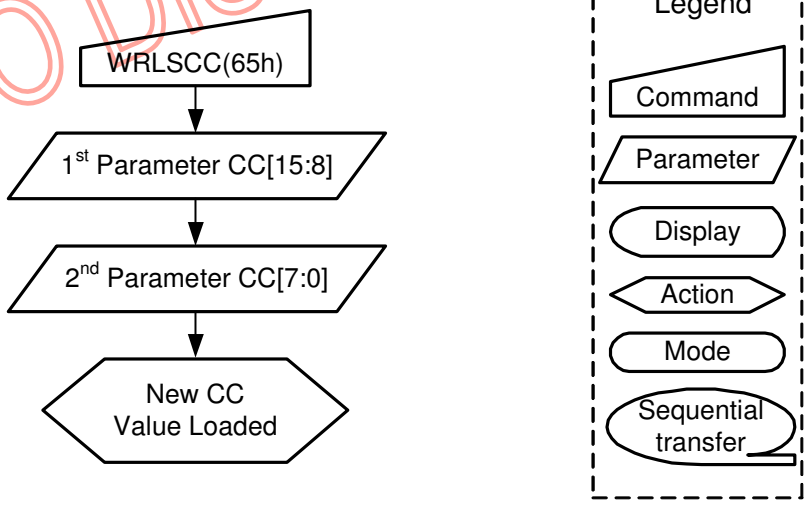
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8000h
S/W Reset	8000h
H/W Reset	8000h

Flow Chart



RDLSCCM: Read Light Sensor Compensation Coefficient Value MSBs (6600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDLSCCM	Write	66h	6600h	00h	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8

NOTE: "-" Don't care

Description

This command returns MSBs of the compensation coefficient value (CC[15:8]) which is stored by "Write Light Sensor Compensation Coefficient Value (6500h)" command.
It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order.
Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "1000 000".

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

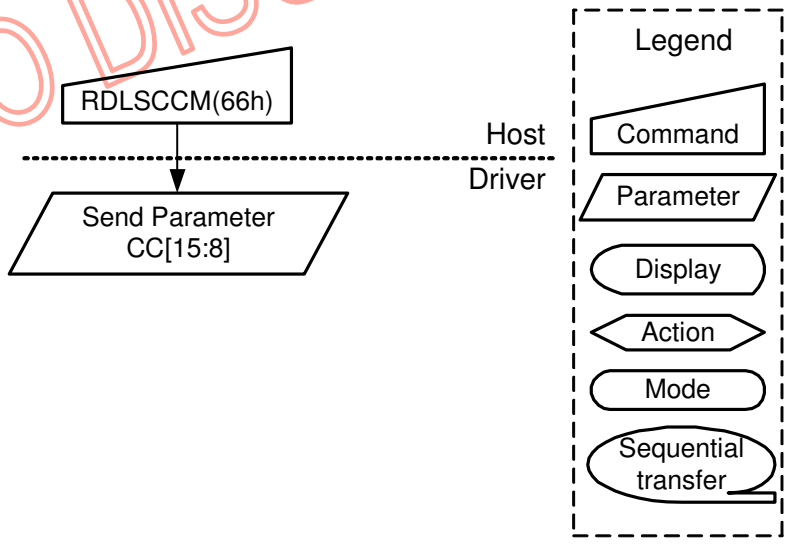
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

Flow Chart



RDLSCCL: Read Light Sensor Compensation Coefficient Value LSBs (6700h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDLSCCL	Write	67h	6700h	00h	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0

NOTE: "-" Don't care

Description

This command returns LSBs of the compensation coefficient value (CC[7:0]) which is stored by "Write Light Sensor Compensation Coefficient Value (6501h)" command.
It can read MSBs/LSBs of "Light Sensor Compensation Coefficient value" with any order.
Default value for compensation coefficient is 1.0 (1000 0000 0000 0000 in binary). MSBs are "0000 000".

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

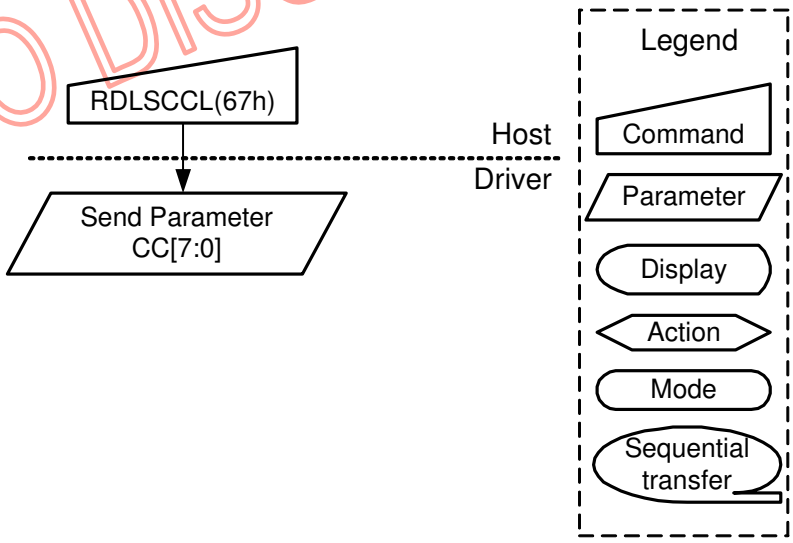
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDBWLB: Read Black/White Low Bits (7000h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBWLB	Read	70h	7000h	00h	Bkx1	Bkx0	Bky1	Bky0	Wx1	Wx0	Wy1	Wy0

NOTE: "-" Don't care

Description

This command returns the lowest bits of black and white color characteristic.
Black: Bkx and Bky
White: Wx and Wy

Restriction

-

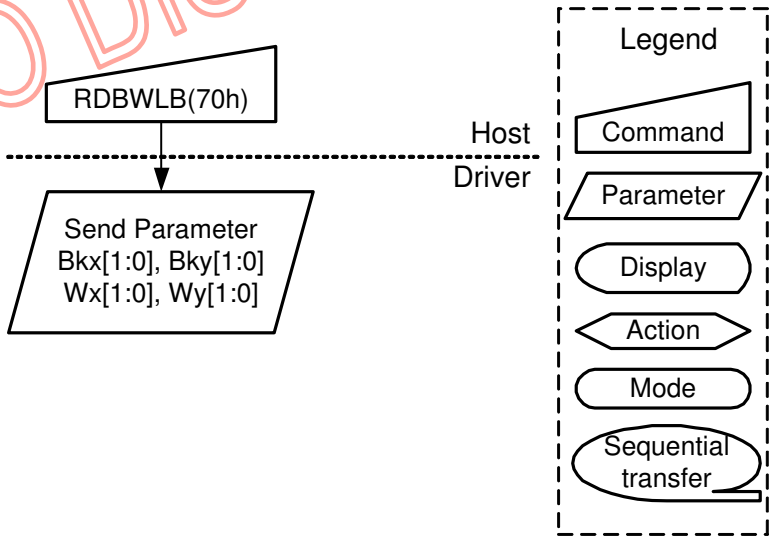
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBkx: Read Bkx (7100h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBkx	Read	71h	7100h	00h	Bkx9	Bkx8	Bkx7	Bkx6	Bkx5	Bkx4	Bkx3	Bkx2

NOTE: "-" Don't care

Description	This command returns the Bkx bit (Bkx[9:2]) of black color characteristic.
Restriction	-

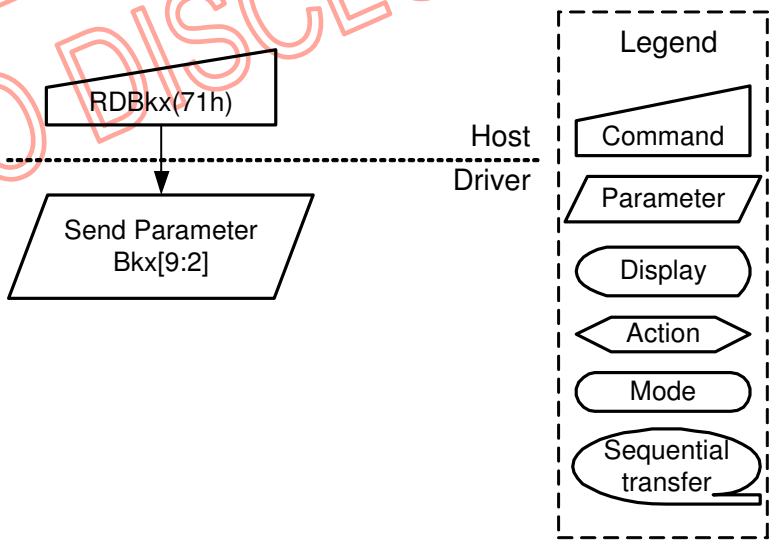
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBky: Read Bky (7200h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBky	Read	72h	7200h	00h	Bky9	Bky8	Bky7	Bky6	Bky5	Bky4	Bky3	Bky2

NOTE: "-" Don't care

Description	This command returns the Bky bit (Bky[9:2]) of black color characteristic.
Restriction	-

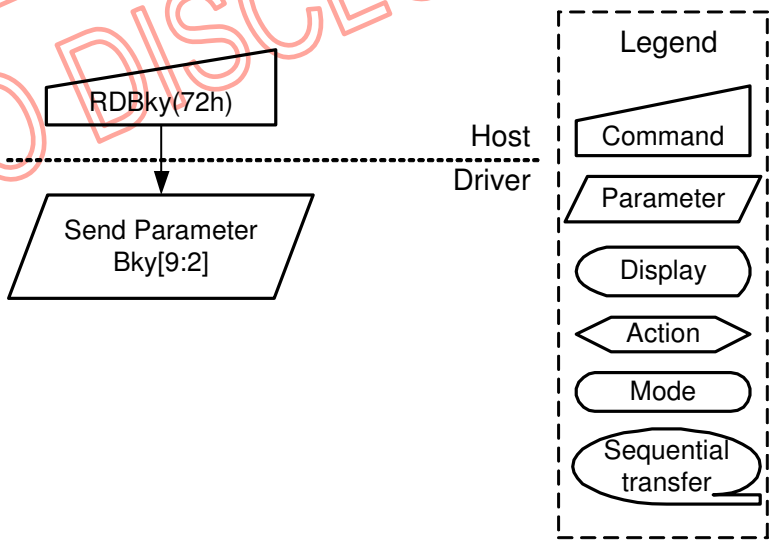
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDWx: Read Wx (7300h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWx	Read	73h	7300h	00h	Wx9	Wx8	Wx7	Wx6	Wx5	Wx4	Wx3	Wx2

NOTE: "-" Don't care

Description	This command returns the Wx bit (Wx[9:2]) of white color characteristic.
Restriction	-

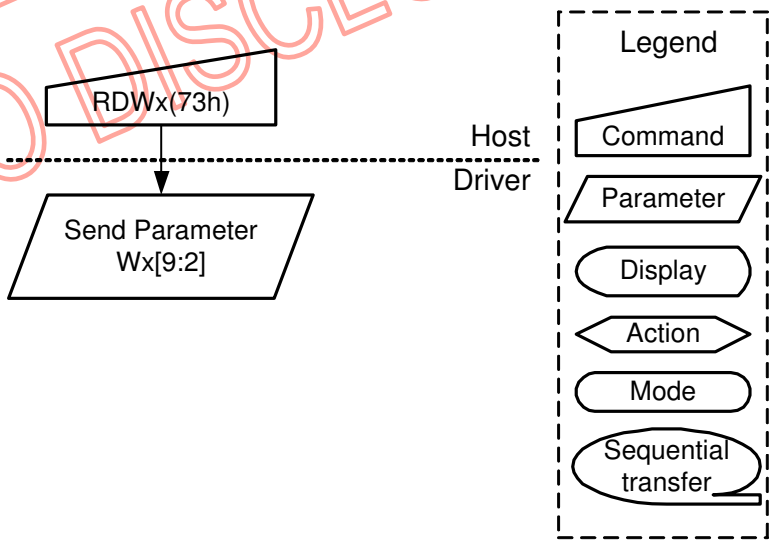
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDWy: Read Wy (7400h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDWy	Read	74h	7400h	00h	Wy9	Wy8	Wy7	Wy6	Wy5	Wy4	Wy3	Wy2

NOTE: "-" Don't care

Description	This command returns the Wy bit (Wy[9:2]) of white color characteristic.
Restriction	-

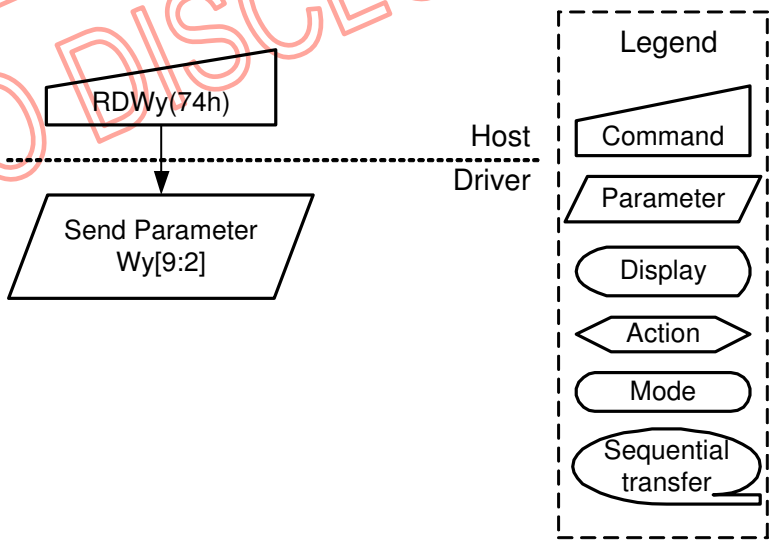
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRGLB: Read Red/Green Low Bits (7500h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRGLB	Read	75h	7500h	00h	Rx1	Rx0	Ry1	Ry0	Gx1	Gx0	Gy1	Gy0

NOTE: "-" Don't care

Description	This command returns the lowest bits of red and green color characteristic. Red: Rx and Ry Green: Gx and Gy
Restriction	-

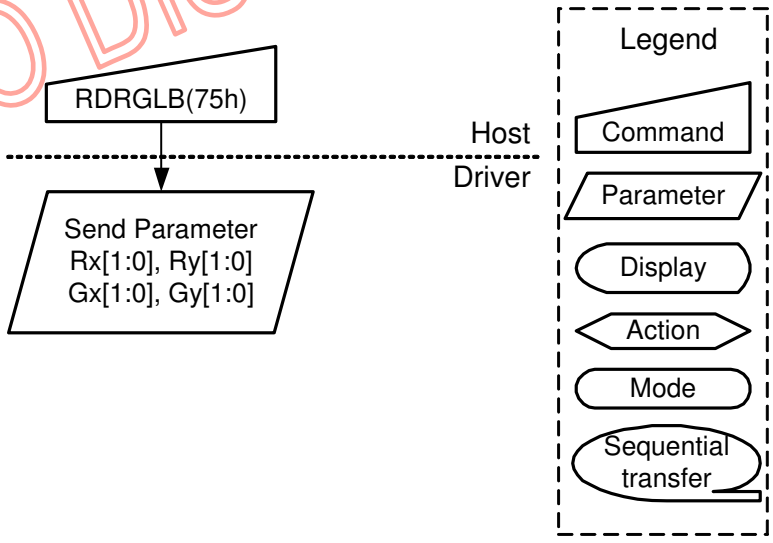
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRx: Read Rx (7600h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRx	Read	76h	7600h	00h	Rx9	Rx8	Rx7	Rx6	Rx5	Rx4	Rx3	Rx2

NOTE: "-" Don't care

Description	This command returns the Rx bit (Rx[9:2]) of red color characteristic.
Restriction	-

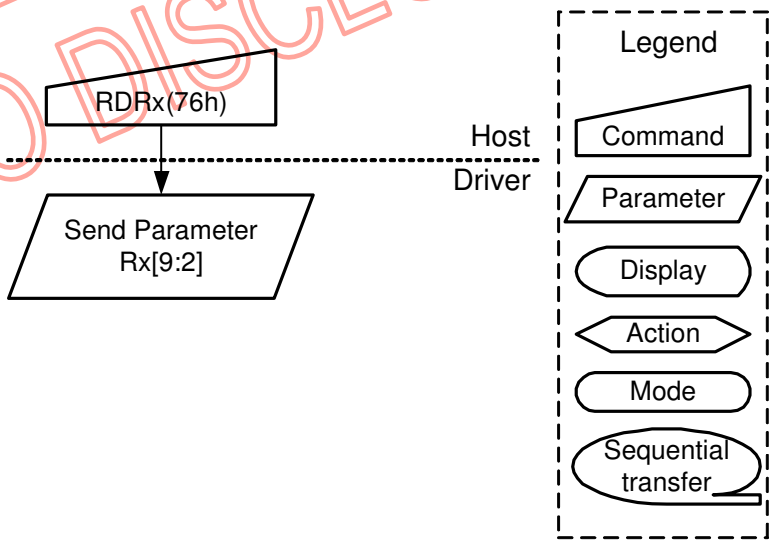
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDRy: Read Ry (7700h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDRy	Read	77h	7700h	00h	Ry9	Ry8	Ry7	Ry6	Ry5	Ry4	Ry3	Ry2

NOTE: "-" Don't care

Description	This command returns the Ry bit (Ry[9:2]) of red color characteristic.
Restriction	-

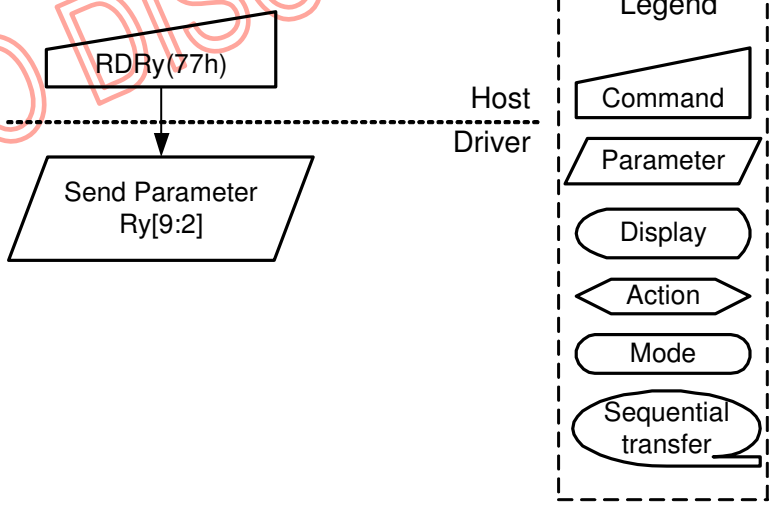
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDGx: Read Gx (7800h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGx	Read	78h	7800h	00h	Gx9	Gx8	Gx7	Gx6	Gx5	Gx4	Gx3	Gx2

NOTE: "-" Don't care

Description	This command returns the Gx bit (Gx[9:2]) of green color characteristic.
Restriction	-

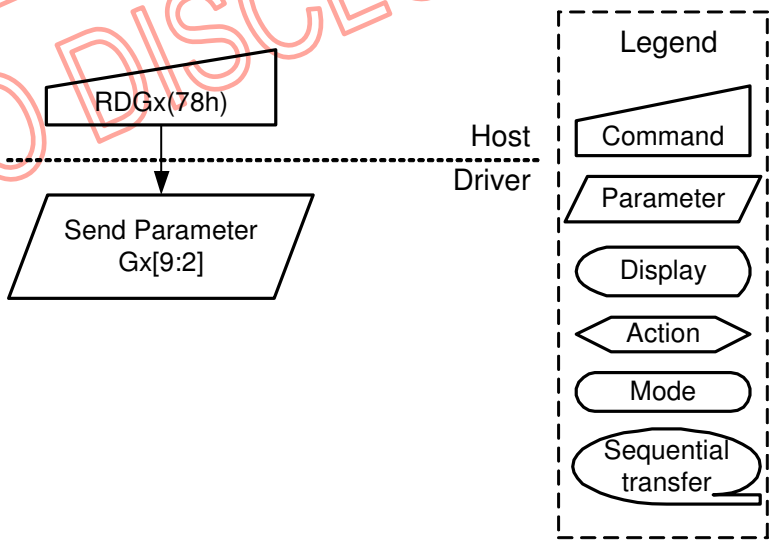
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDGy: Read Gy (7900h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDGy	Read	79h	7900h	00h	Gy9	Gy8	Gy7	Gy6	Gy5	Gy4	Gy3	Gy2

NOTE: "-" Don't care

Description	This command returns the Gy bit (Gy[9:2]) of green color characteristic.
Restriction	-

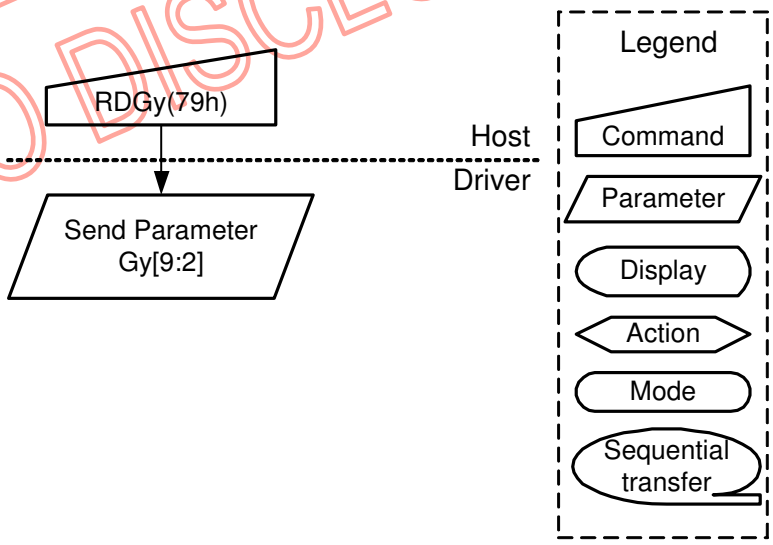
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBALB: Read Blue/AColor Low Bits (7A00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBALB	Read	7Ah	7A00h	00h	Bx1	Bx0	By1	By0	Ax1	Ax0	Ay1	Ay0

NOTE: "-" Don't care

Description	This command returns the lowest bits of blue and A color characteristic. Blue: Bx and By A: Ax and Ay
Restriction	-

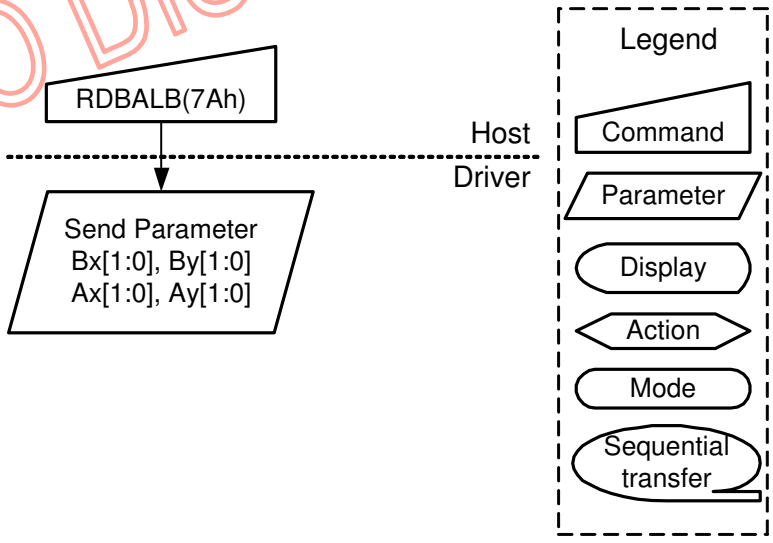
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBx: Read Bx (7B00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBx	Read	7Bh	7B00h	00h	Bx9	Bx8	Bx7	Bx6	Bx5	Bx4	Bx3	Bx2

NOTE: "-" Don't care

Description	This command returns the Bx bit (Bx[9:2]) of blue color characteristic.
Restriction	-

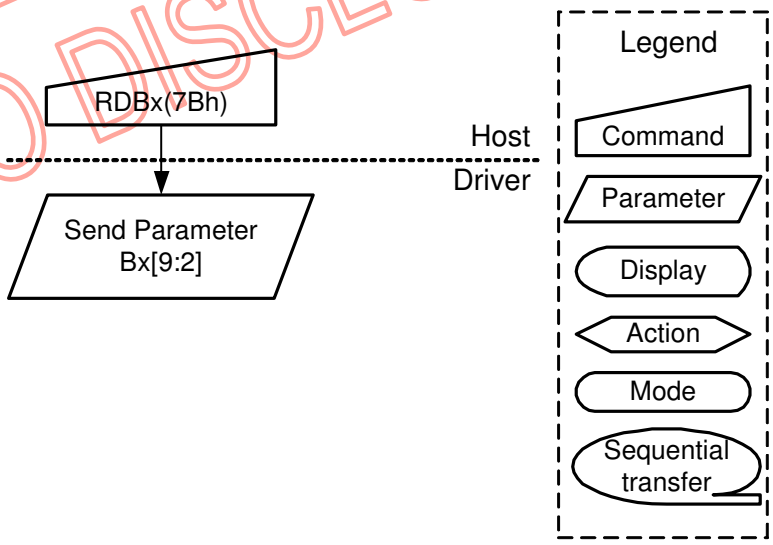
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDBy: Read By (7C00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDBy	Read	7Ch	7C00h	00h	By9	By8	By7	By6	By5	By4	By3	By2

NOTE: "-" Don't care

Description	This command returns the By bit (By[9:2]) of blue color characteristic.
Restriction	-

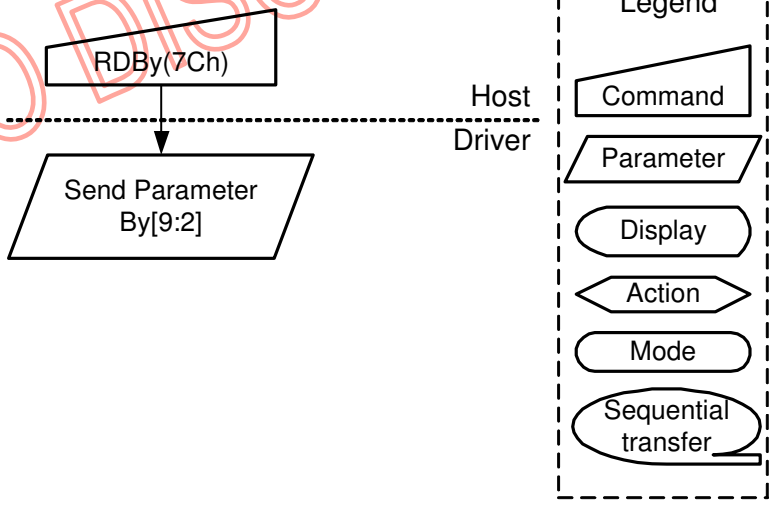
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDAx: Read Ax (7D00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAx	Read	7Dh	7D00h	00h	Ax9	Ax8	Ax7	Ax6	Ax5	Ax4	Ax3	Ax2

NOTE: "-" Don't care

Description	This command returns the Ax bit (Ax[9:2]) of A color characteristic.
Restriction	-

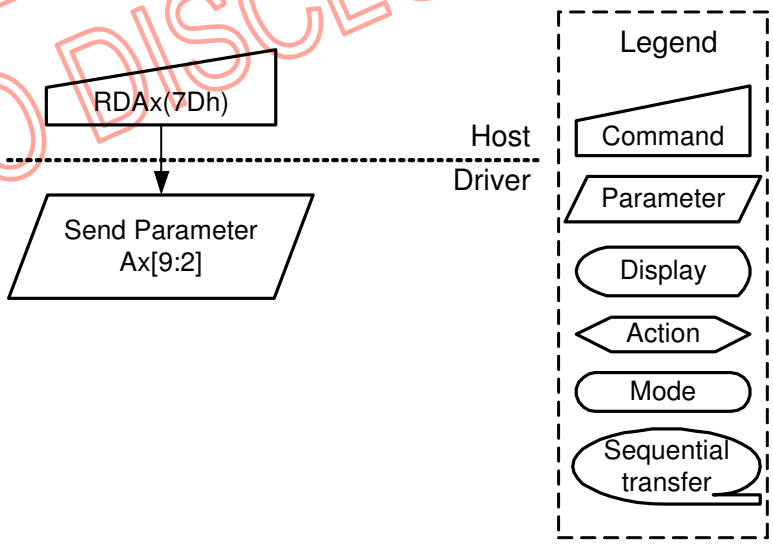
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDAy: Read Ay (7E00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDAy	Read	7Eh	7E00h	00h	Ay9	Ay8	Ay7	Ay6	Ay5	Ay4	Ay3	Ay2

NOTE: "-" Don't care

Description	This command returns the Ay bit (Ay[9:2]) of A color characteristic.
Restriction	-

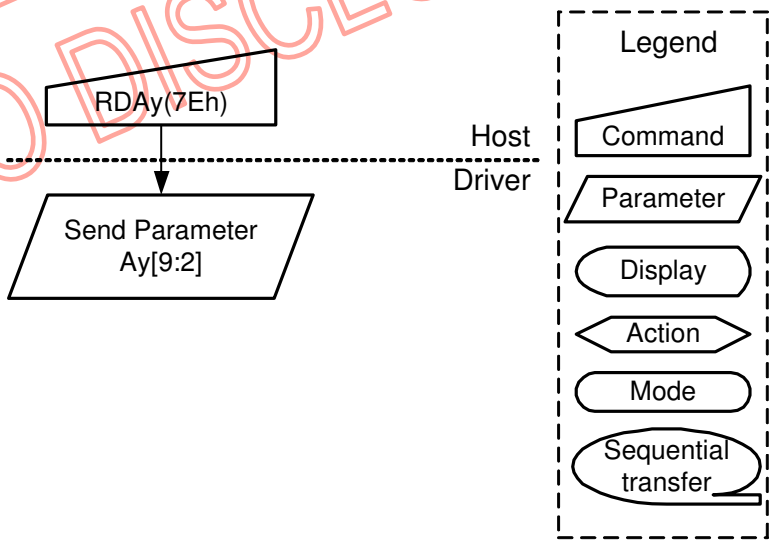
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDDDBS: Read DDB Start (A100h~A104h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDDBS	Read	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
			A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A104h	00h	1	1	1	1	1	1	1	1

NOTE: "-" Don't care

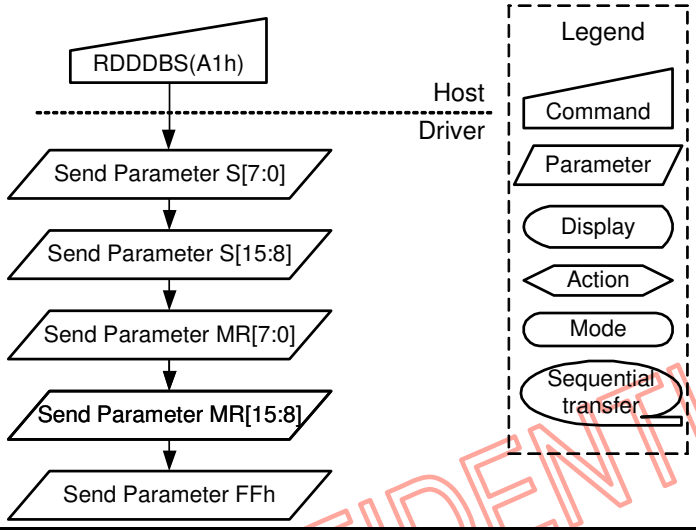
Description	This command returns the supplier identification and display module mode/revision information. *Note: This information is not the same what "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands are returning.* *Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.* This read sequence can be interrupted by any command and it can be continued by "Read DDB Continue (A8h)" command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent. SID[15:0]: Supplier identification MID[15:0]: Module ID
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDDDBC: Read DDB Continue (A800h~A804h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDDBC	Read	A8h	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0
			A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8
			A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0
			A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8
			A804h	00h	1	1	1	1	1	1	1	1

NOTE: "-" Don't care

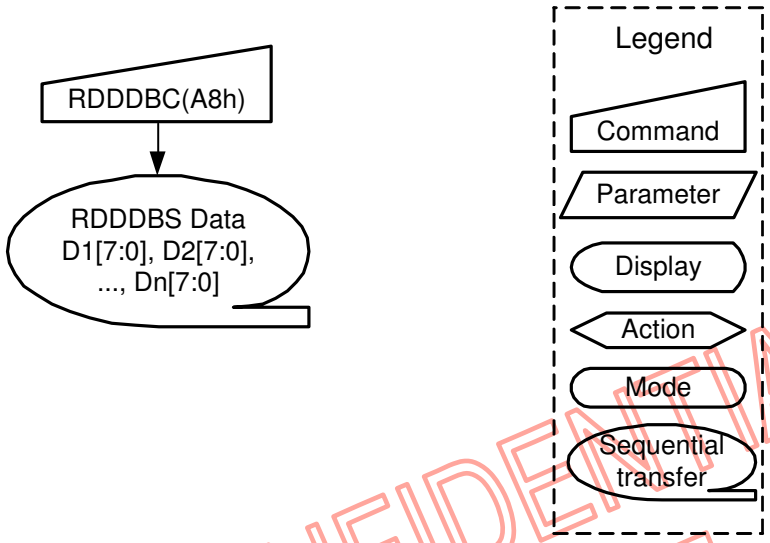
Description	This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command. *Note: Parameter 0xFF is an "Exit Code", this means that there is no more data in the DDB block.* *Note: For use example,* *1. Set maximum return packet size=3* *2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0]* *3. Read 0xA8, return 2 bytes MID[15:8] and 0xFF*
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDFCS: Read First Checksum (AA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDFCS	Read	AAh	AA00h	00h	FCS7	FCS6	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0

NOTE: "-" Don't care

Description	This command returns the first checksum what has been calculated from "User Command Set" area registers (not include "Manufacture Command Set) and the frame memory after the write access to those registers and/or frame memory has been done.
Restriction	It will be necessary to wait 150ms after there is the last write access on "User Command Set" area registers before there can read this checksum value.

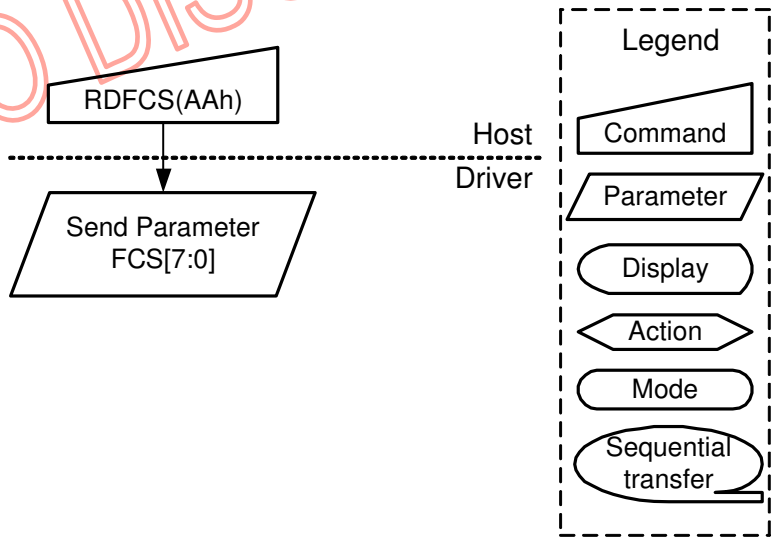
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDCCS: Read Continue Checksum (AF00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDCCS	Read	AFh	AF00h	00h	CCS7	CCS6	CCS5	CCS4	CCS3	CCS2	CCS1	CCS0

NOTE: "-" Don't care

Description

This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from "User Command Set" area registers and the frame memory after the write access to those registers and/or frame memory has been done.

Restriction

It will be necessary to wait 300ms after there is the last write access on "User Command Set" area registers before there can read this checksum value in the first time.

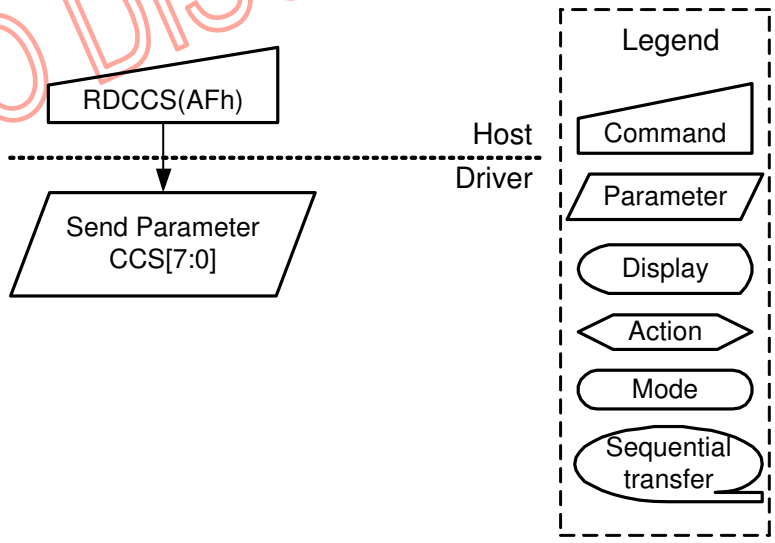
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



RDID1: Read ID1 Value (DA00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

NOTE: "-" Don't care

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-

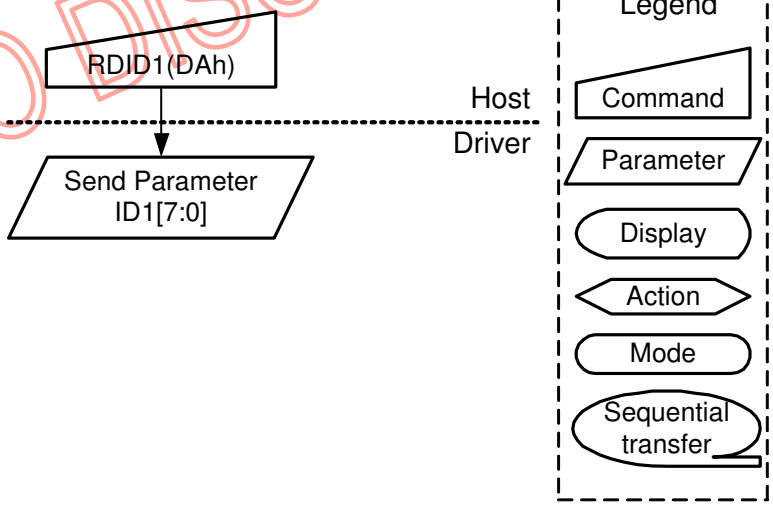
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



RDID2: Read ID2 Value (DB00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

NOTE: "-" Don't care

Description	This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 80h to FFh
Restriction	-

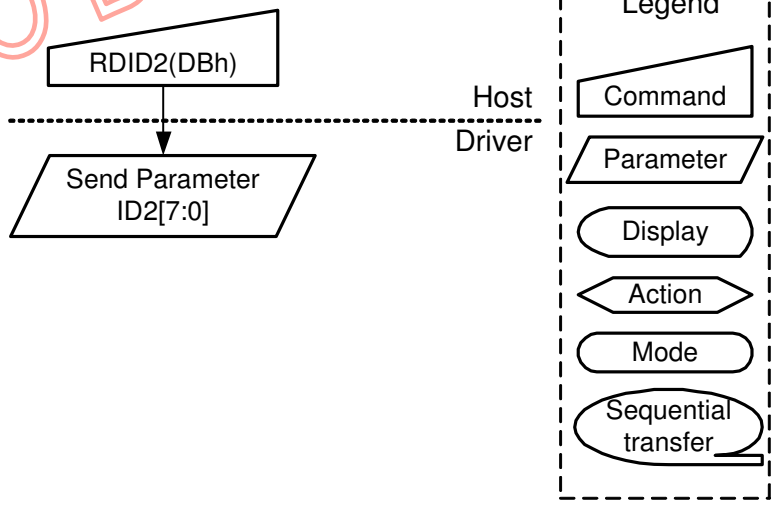
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	80h
S/W Reset	MTP Value	80h
H/W Reset	MTP Value	80h

Flow Chart



RDID3: Read ID3 Value (DC00h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Others	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

NOTE: "-" Don't care

Description	This parameter read byte identifies the TFT LCD module/driver.
Restriction	-

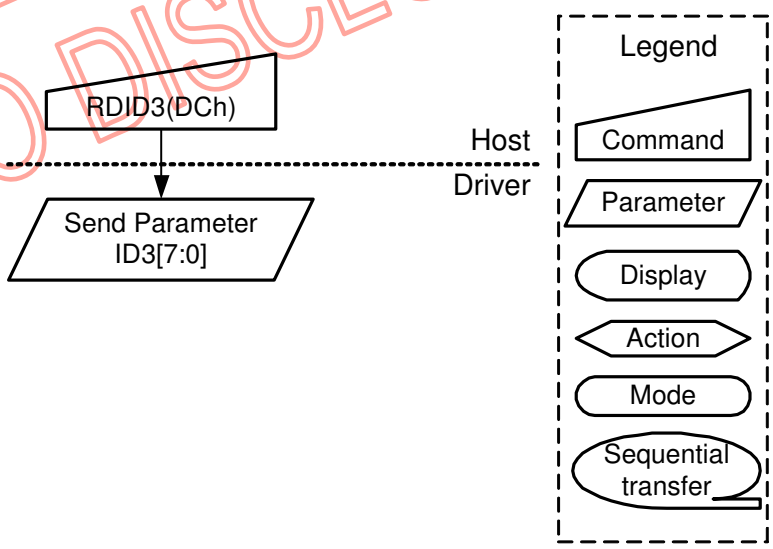
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	After MTP	Before MTP
Power On Sequence	MTP Value	00h
S/W Reset	MTP Value	00h
H/W Reset	MTP Value	00h

Flow Chart



7 REFERENCE APPLICATIONS

7.1 Microprocessor Interface

The display, which is using 80-series MPU interface, is connected to the MPU as it is illustrated below.

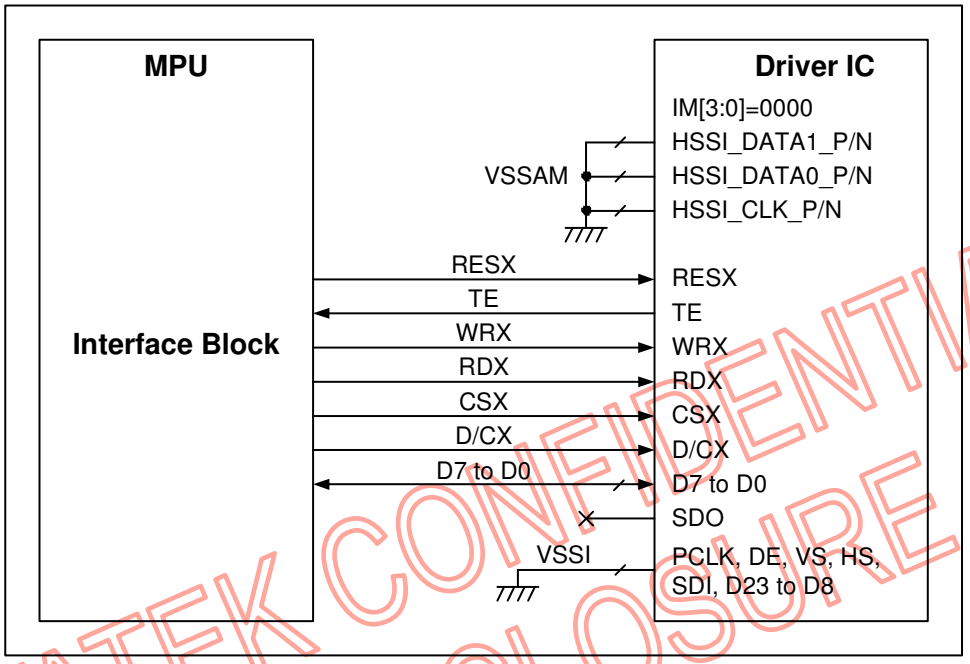


Fig. 7.1.1 Interfacing for 80-series 8-bit MPU by Connecting IM[3:0]="0000"

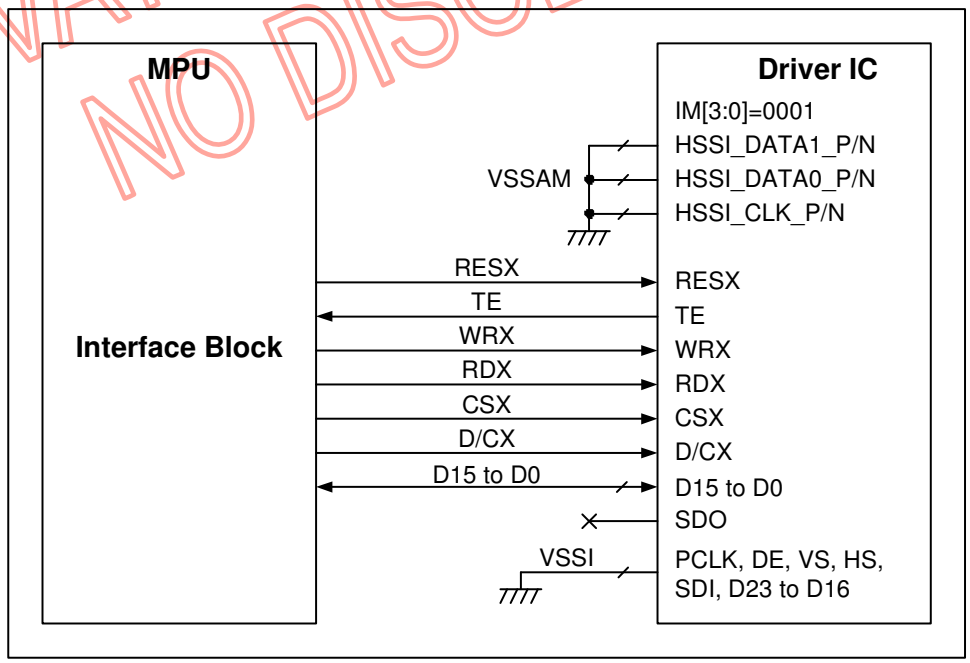


Fig. 7.1.2 Interfacing for 80-series 16-bit MPU by Connecting IM[3:0]="0001"

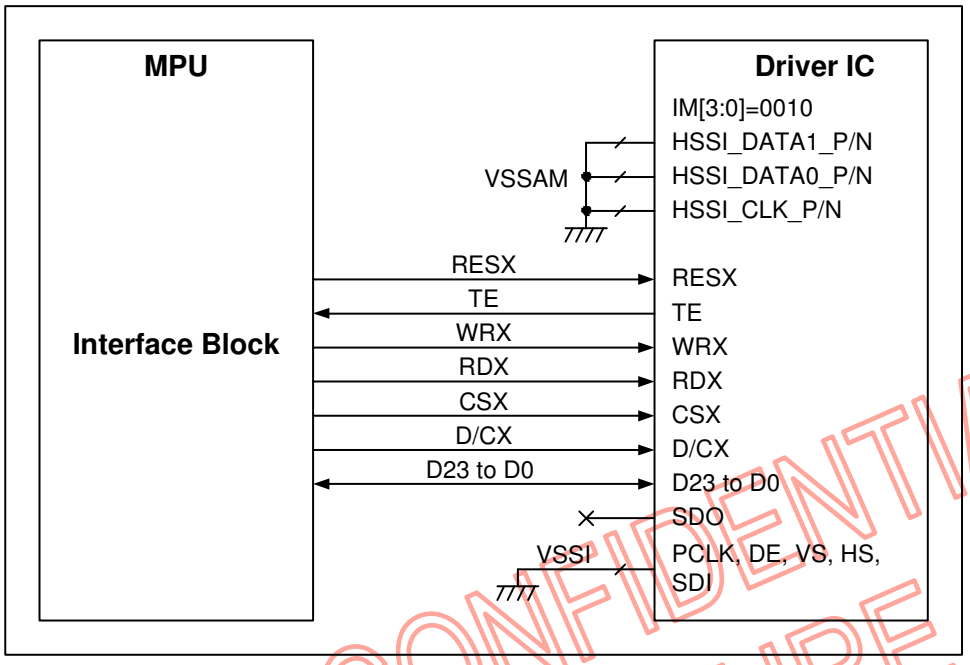


Fig. 7.1.3 Interfacing for 80-series 24-bit MPU by Connecting IM[3:0]="0010"

Note: Left MVDDL and MVDDA open (not used) when using 80-series MPU interface.

The display, which is using RGB with 16-bit SPI interface, is connected to the MPU as it is illustrated below.

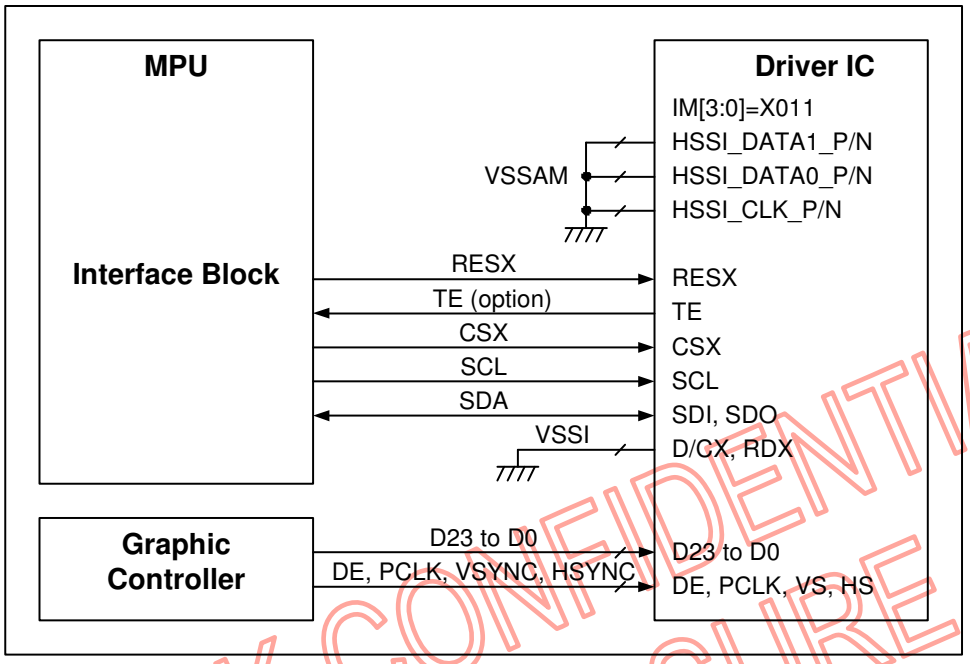


Fig. 7.1.4 Interfacing for RGB with SPI by Connecting IM[3:0]="X011"

The display, which is using RGB with I2C interface, is connected to the MPU as it is illustrated below.

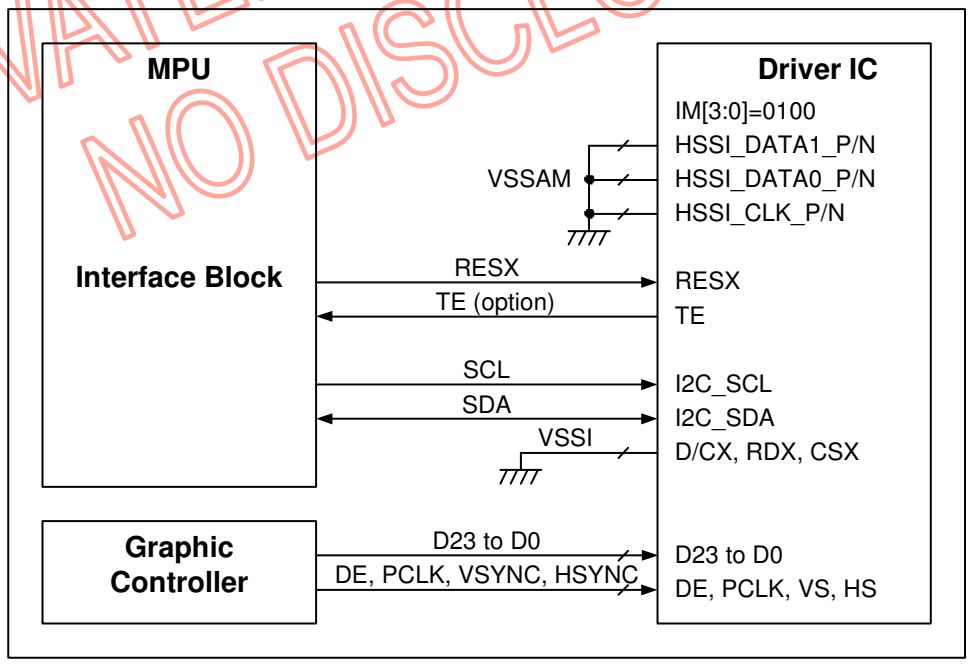


Fig. 7.1.5 Interfacing for RGB with I2C by Connecting IM[3:0]="0100"

Note 1. Connecting D23, D22, D15, D14, D7 and D6 to VSSI when using 18-bit/pixel (VIPF[3:0]="0110").
Connecting D23~D21, D15, D14 and D7~ D5 to VSSI when using 16-bit/pixel (VIPF[3:0]="0101").
Note 2. Left MVDDL and MVDDA open (not used) when using RGB with SPI interface.
Note 3. IM3 is used to select SCL rising or falling edge trigger for 16-bit SPI interface.

The display, which is using MIPI DSI and the TE line, is connected to the MPU as it is illustrated below.

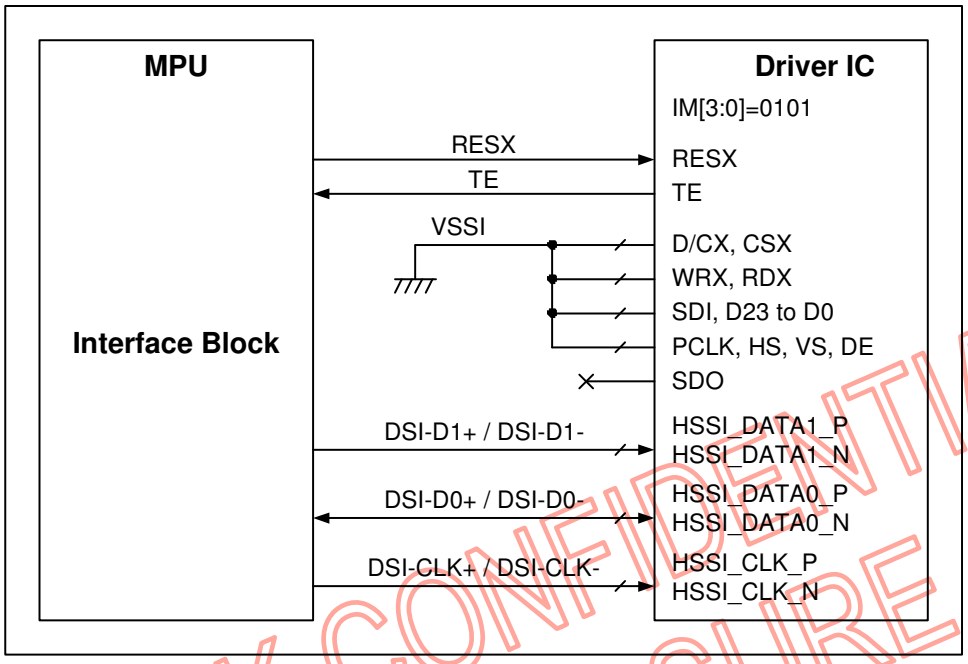


Fig. 7.1.6 Interfacing for MIPI DSI with TE Line by Connecting IM[3:0]="0101"

The display, which is using MIPI DSI without the TE line, is connected to the MPU as it is illustrated below.

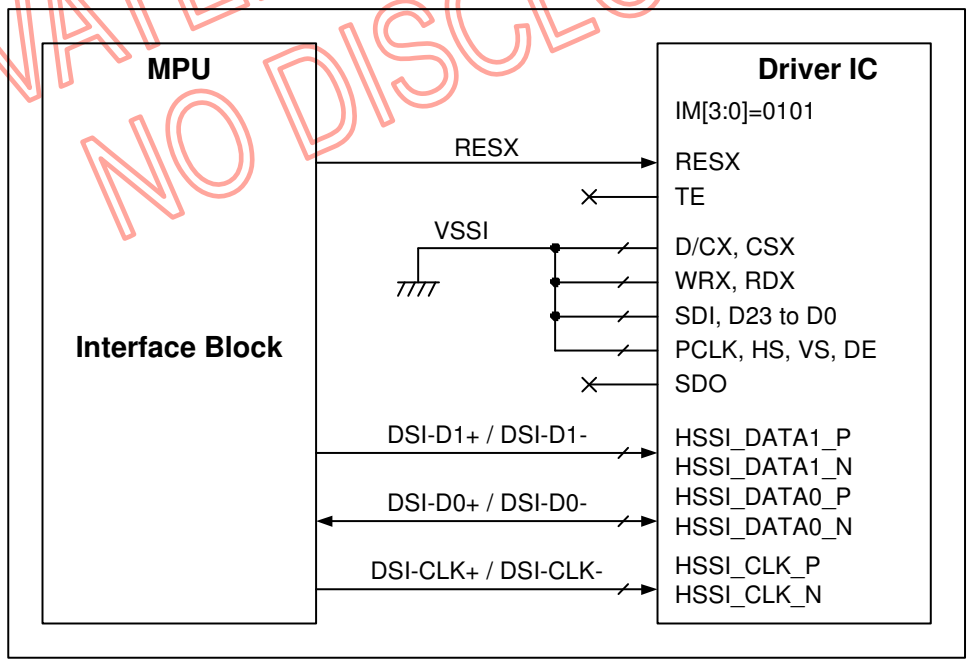


Fig. 7.1.7 Interfacing for MIPI DSI without TE Line by Connecting IM[3:0]="0101"

Note1. Bit DSITE should be "1", the TE line is enabled, when using MIPI with TE line.
Note2. Bit DSITE should be "0", the TE line is disabled, when using MIPI without TE line. The command 35h TEON cannot active the separated TE line.
Note3. Connecting HSSI_DATA1_P/N to VSSAM when using 1 data lane application.

The display, which is using MDDI with 16-bit SPI interface, is connected to the MPU as it is illustrated below.

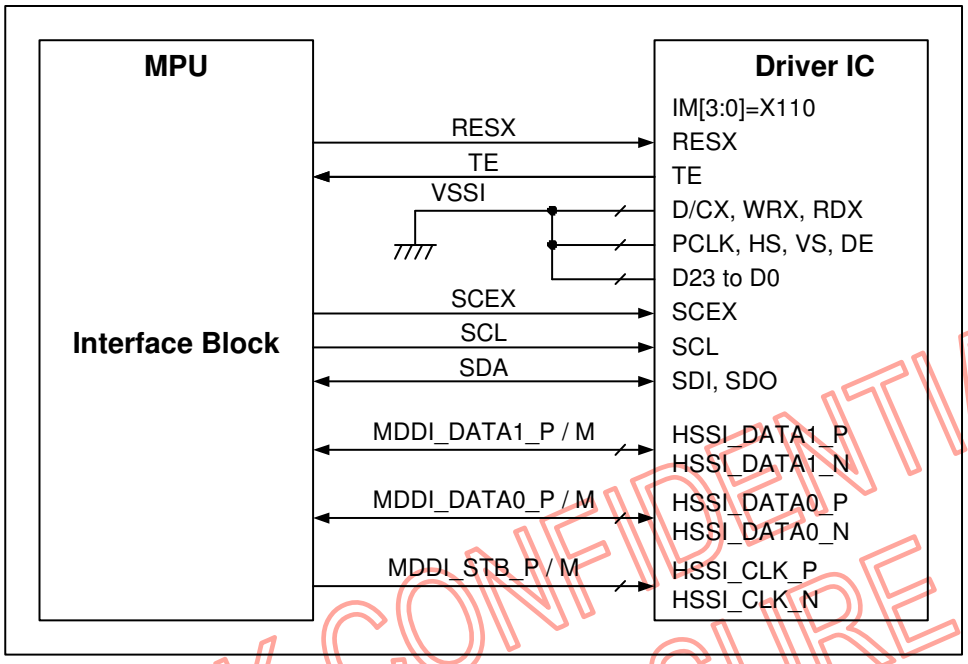


Fig. 7.1.8 Interfacing for MDDI with 16-bit SPI by Connecting IM[3:0]="X110"

The display, which is using MDDI with I2C interface, is connected to the MPU as it is illustrated below.

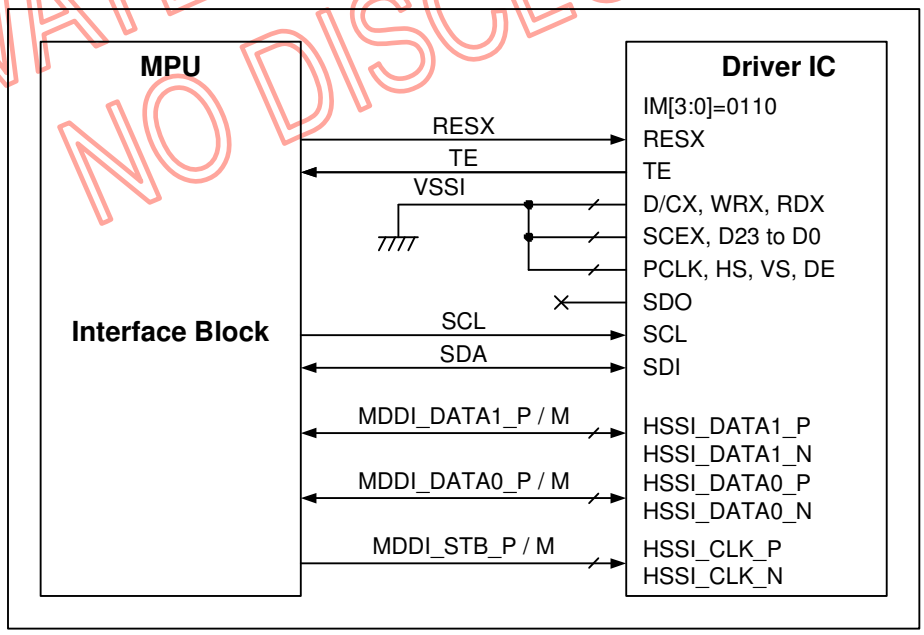
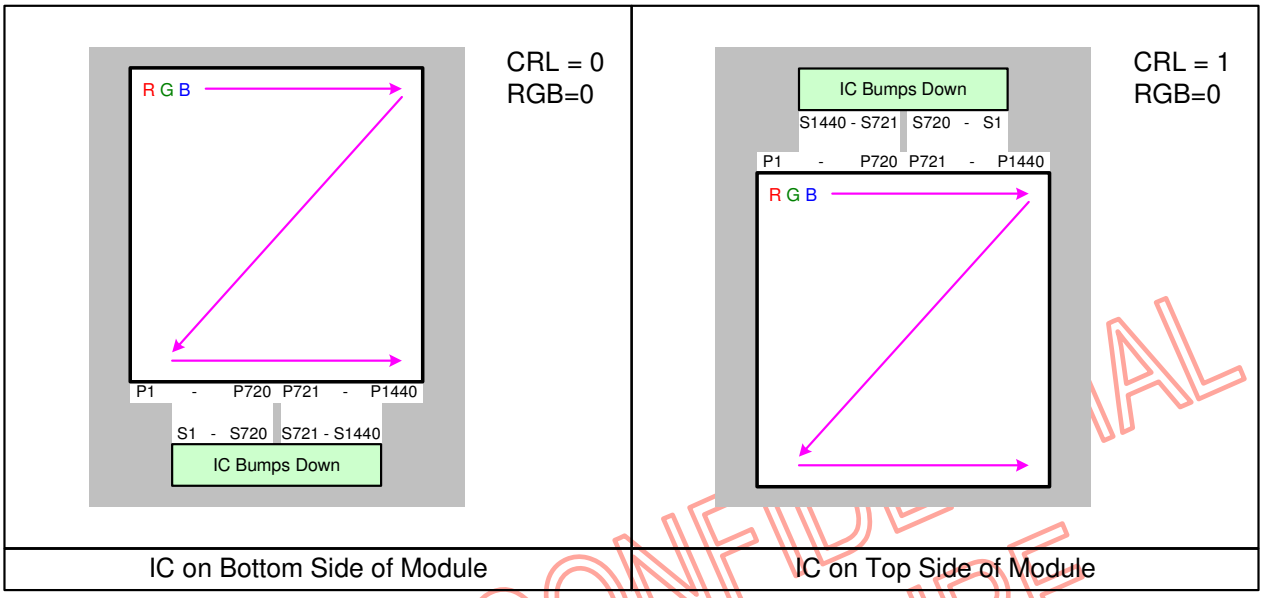


Fig. 7.1.9 Interfacing for MDDI with I2CI by Connecting IM[3:0]="0111"

Notes:
1. Connecting HSSI_DATA1_P/N to VSSAM when using MDDI Type-I (1 data lane).
2. IM3 is used to select SCL rising or falling edge trigger when using 16-bit SPI interface.

7.2 Connections with Panel



NOTES:
1. The scan direction from top to bottom indicated in above figure means (CTB XOR ML = "0").
2. The relationship between Sn output sequence and CRL/CGM[7:0] is shown below.

CGM[7:0]	Display Resolution	Sn Output Sequence	Note
70h	480RGB x 864	CRL="0": $S1_{(R)}$→$S2_{(G)}$→$S3_{(B)}$→…→$S1438_{(R)}$→$S1439_{(G)}$→$S1440_{(B)}$ CRL="1": $S1440_{(R)}$→$S1439_{(G)}$→$S1438_{(B)}$→…→$S3_{(R)}$→$S2_{(G)}$→$S1_{(B)}$	All S1 to S1440 are used
6Bh	480RGB x 854		
50h	480RGB x 800		
28h	480RGB x 720		
00h	480RGB x 640		